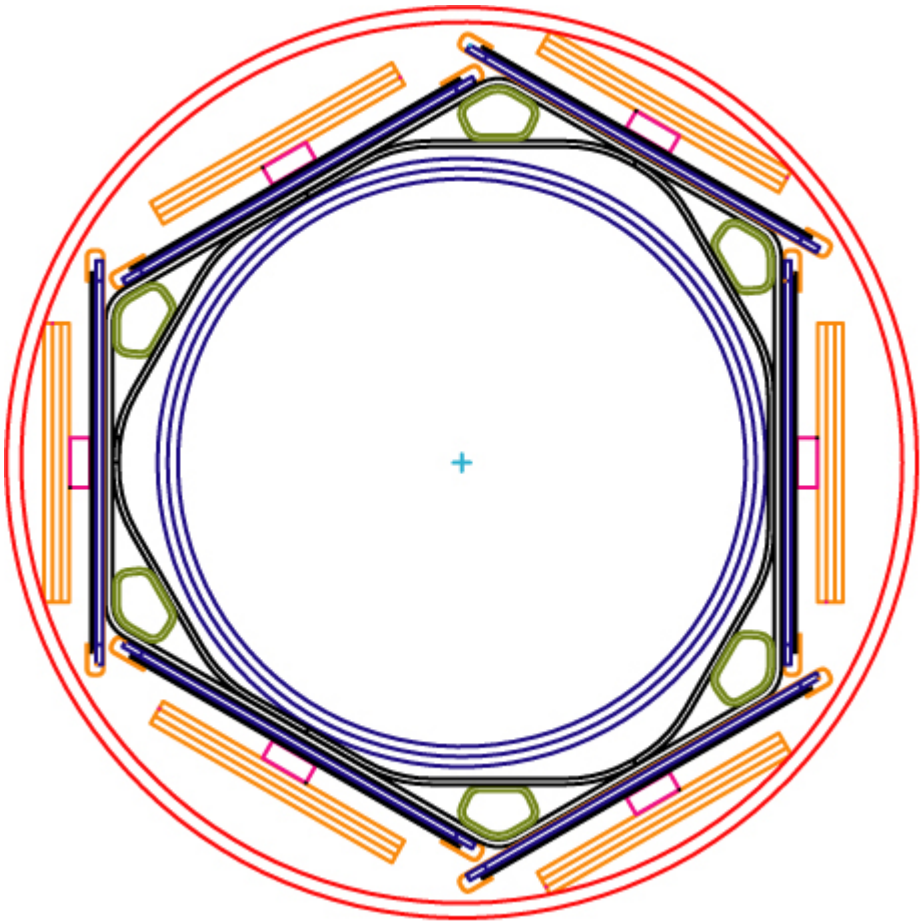
DØ Layer 0
Conceptual
Design Report



LAYER Ø
SILICON DETECTOR

DRAFT
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1 INTRODUCTION

The current DØ silicon microstrip tracker was built to withstand the 2 to 4 fb^{-1} of integrated luminosity originally projected for Run II. The recently updated design goals for Run II accelerator operations[1] open the possibility that a total integrated luminosity of 8 fb^{-1} may be delivered to the collider experiments. This large integrated luminosity will render the inner layers of the present silicon tracker inoperable due to radiation damage. Of particular importance to be able to exploit the physics potential of the Tevatron is the ability to tag b-jets. The proposed addition of a single inner layer silicon detector to the current silicon microstrip tracker should improve the impact parameter resolution of the tracker and allow DØ to retain and strengthen its physics capabilities in spite of the ravages of radiation damage upon the currently installed detector. The addition of this Layer 0 detector should also help maintain pattern recognition capabilities for higher pseudorapidity tracks.

Based upon the originally anticipated luminosity potential of Run IIb, the DØ collaboration had proposed an upgraded silicon tracker[2] that would occupy the location of the current silicon microstrip tracker. That project was approved, and technically very advanced.[3] Most prototyping efforts had been completed when the director decided to terminate the Run IIb silicon upgrade.[4] The collaboration now proposes to build a new silicon detector, Layer 0, to be installed inside the current silicon microstrip tracker. The design of this Layer 0 detector relies heavily on the work performed for the Run IIb detector. The Layer 0 detector will consist of a carbon fiber support structure mounted on the beam tube. To minimize material in the silicon sensor region and address the stringent cooling constraints, the silicon sensors will be connected to readout chips via analog cables. Extensive prototyping has been done on low mass, fine pitch, flexible cables for Run IIb, which was highly successful. Readout will employ the new SVX4 readout chip developed for Run IIb. The SVX4 chips are mounted on ceramic hybrids outside the tracking volume on an extended carbon fiber support structure. It is anticipated that the hybrid design for the Run IIb detector can be carried over to the Layer 0 detector. All downstream electronics is nearly identical to the Run IIb design. Extensive radiation tests were performed on prototype innermost sensors for the Run IIb detector and those were found to survive the radiation damage associated with the original projected Run IIb accelerator performance, which called for delivering 15 fb^{-1}. It is anticipated that the Layer 0 detector can be installed in the current silicon microstrip tracker within a period of 8 weeks, including commissioning.

This report describes the conceptual design of a new Layer 0 silicon detector for the DØ experiment to be installed inside the current silicon tracker during a future accelerator shutdown. The Run IIb proposal also called for an inner layer silicon detector at about the same radius. The prototyping for that project was quite mature, and the following chapters include some information based upon those developments. Section 2 provides an overview of the proposed DØ layer 0 silicon detector design and serves as an introduction to the following sections. Section 3

[1] http://www-bd.fnal.gov/doereview03/docs/Overview7.1.pdf
[2] DØ Run IIb Upgrade Technical Design Report, FERMILAB-PUB-02-327-E, December 2002.
[3] See the following web page for a summary of Run IIb silicon project status as of August 2003
http://D0server1.fnal.gov/projects/run2b/Meetings/DOEReviews/Aug03_Update/Aug03_update_web.htm
[4] http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/Detector_upgrade_decision.pdf

discusses the silicon sensors, Section 4 the mechanical aspects of the design, and Section 5 the readout electronics. Section 6 describes the production and testing and Section 7 describes temperature and radiation monitoring. The software requirements for this detector are identical to the software requirements for the Run IIb detector. As such, reference is made to the software needed for the quality assurance and testing of the devices in Section 8. Section 9 briefly presents some results of simulation studies to determine the expected detector performance.

2 LAYER 0 SILICON DETECTOR DESIGN

2.1 Introduction

The Layer 0 silicon detector design is based on an optimization of the physics performance of the detector while at the same time satisfying various stringent boundary conditions, both external and internal. The most obvious boundary condition to be satisfied is that the new detector has to fit within the current Run IIa silicon detector. Moreover, installation of the new detector has to proceed with minimal risk of damaging the current and new detector. Interfacing the new detector within the existing framework, notably the trigger framework, sets internal constraints.

To maximize the physics benefits from the Layer 0 detector, it should be installed as soon as is feasible. This argues for a simple design requiring minimal prototyping. To minimize prototyping, schedule risk and incremental costs of the project, the design should utilize Run IIb Silicon Upgrade R&D results where possible.

The remainder of this section will describe in more detail the external constraints on the detector and introduce its basic design features.

2.2 Design Constraints

The geometry of the currently installed detector severely constrains the Layer 0 detector, and details of those constraints are found in section 4.2.

2.2.1 Radiation environment

The collaboration embarked on radiation studies of silicon sensors for both the present and proposed Run IIb detector to determine the operating parameters for the Run IIb detector. The results of these studies are directly applicable to the Layer 0 detector. Based on these measurements, and parameters obtained by other experiments, simulation studies were carried out of the leakage current, depletion voltage, and equivalent noise to determine the silicon operating temperature and to ensure that the device can withstand the foreseen accumulated dose. It was determined that operating the detector within the same environment as the current silicon, with the inlet cooling temperature at –8 degrees Celsius, is adequate. We also determined that a minimum radius of about 15 mm for the innermost layer of silicon should provide an adequate safety margin for running the detector to integrated luminosities of 8 fb^{-1}.

2.2.2 Silicon track trigger

The Run IIa silicon detector employs a Silicon Track Trigger (STT) that processes data from the Level 1 Central Track Trigger (CTT) and the silicon tracker. It associates hits in the silicon with tracks found by the Level 1 CTT. These hits are then fit together with the Level 1 CTT information, thus improving the resolution in momentum and impact parameter, and the rejection of fake tracks. The STT has three types of electronics modules:

- The Fiber Road Card (FRC), which receives the data from CTT and fans them out to the other modules.

- The Silicon Trigger Card (STC), which receives the raw data from the silicon tracker front end. It processes the data to find clusters of hit strips that are associated with the tracks found by the CTT. Each card accepts input from at most eight readout hybrids.

- The Track Fit Card (TFC), which fits a trajectory to the CTT tracks and the silicon clusters associated with it. These results are relayed to the Level 2 Central Track Trigger. Each card can accept at most eight STC inputs.

The trigger makes use of a 6-fold ϕ-symmetry. The STT modules are located in 6 VME crates, each serving two 30-degree azimuthal sectors. Currently each of these crates holds one FRC, nine STCs, and two TFCs - one per 30-degree sector. Each crate can hold at most 12 STCs, with a possibility to go to 16 STC cards with a redesigned backplane. It is these constraints that favor a design with 6-fold, or integer multiple of 6-fold, symmetry.

2.2.3 Cable plant

The total number of readout modules in the new system is constrained by the currently available cable plant, which allows for about 940 cables. No new cables can be added to the existing cable plant. There simply is not enough space between the central and end calorimeters to route more cables. The current detector has 912 readouts. Some of the spare channels are taken due to defective components in the existing cable plant. The new detector calls for an additional 48 readouts. These cannot be accommodated in the current system without disconnecting existing readout modules. It might be argued that the cables of the dead modules could be used for the Layer 0 detector. The location of these dead channels on the adapter card ring make routing nearly impossible and make this a non-viable option. Therefore, it is proposed to disconnect cables from at least some of the H-disks, which would allow a maximum of 96 cables for the Layer 0 detector. These cables are conveniently located on the adapter card ring on the face of the central calorimeter, and allow for an effective cabling.

2.3 Baseline Design Overview

The proposed silicon detector has a single layer geometry arranged in a barrel design. It is envisioned that the detector will be built as one unit. One type of highly radiation tolerant sensor is foreseen with two different lengths. The sensors will have axial readout only with intermediate strips. Figure 1 shows an axial view of the Layer 0 detector. The emphasis is on obtaining improved impact parameter resolution in the R-ϕ plane and strengthening the pattern recognition. The design has a 6-fold geometry. The sensors will be mounted on a carbon fiber support structure, which is supported from the beam tube. The sensors will be located at a radius of about 17 mm. These sensors will have 256 channels and a pitch of 70 to 75 μm. The main space constraints are imposed by requirements on radial clearance to the beam tube and to the opening in the existing silicon support structures in the installed Run IIa detector. These are described in detail below. The new Layer 0 detector, with the inner support structure and outer screen, must reside in $16.0 < R < 22.0$ mm.

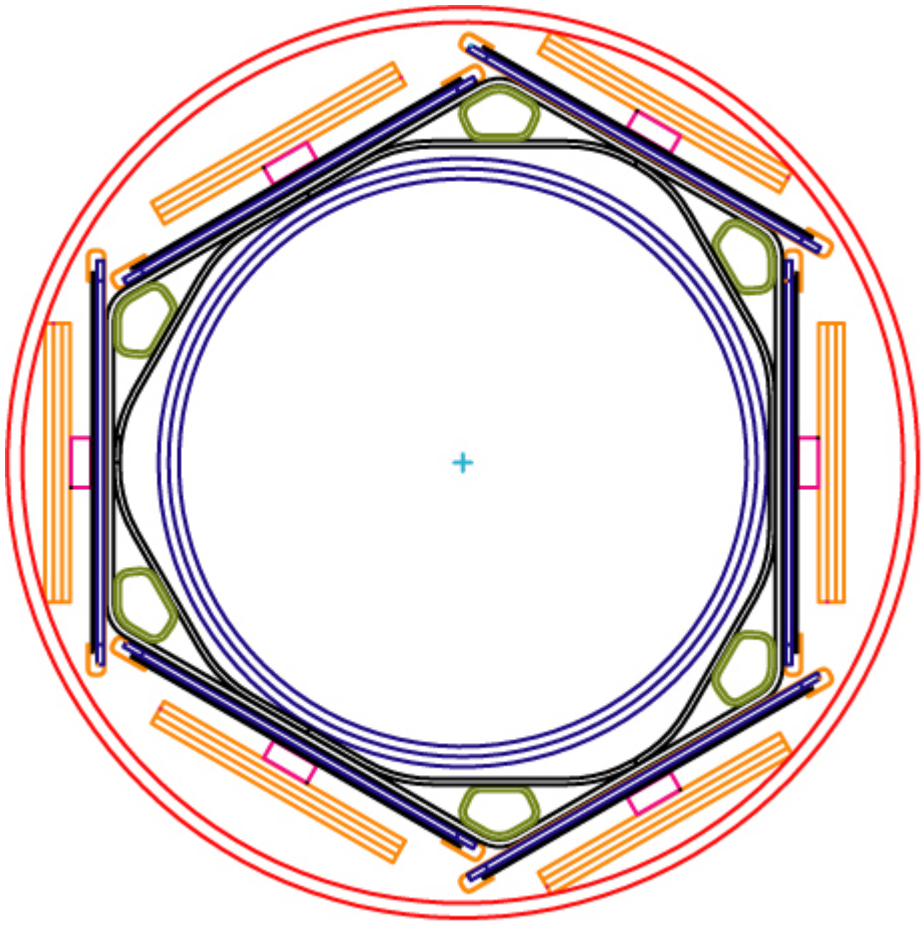

Figure 1 - Axial view of the proposed Layer 0 detector. This layer will provide an additional axial track measurement. The readout uses analog low mass cables which connect to hybrids outside of the active region.

Because of the tight space constraints, the cooling requirements for the innermost layer, and to minimize the amount of material, no readout electronics will be mounted on the sensors, *i.e.* this layer will have 'off-board' electronics. Analog cables will be wirebonded to the sensors, carrying the analog signals to a hybrid where the signals will be digitized and sent to the data acquisition system. Keeping the hybrid mass out of the detector active region also helps in reducing photon conversions. A major challenge in designing the mechanical structure for this layer is ensuring that it fits within the current silicon detector and can be installed without risk of damaging either. Figure 2 shows the current silicon detector in which the new detector will be inserted. The beam tube will be replaced with a new, smaller diameter beam tube.

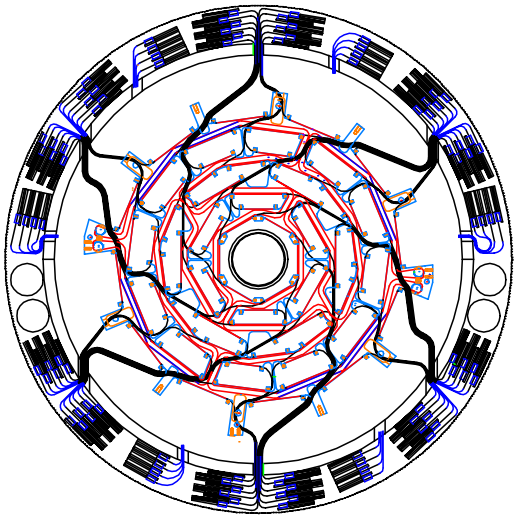

Figure 2 - Axial view of the current silicon detector. The innermost layer resides at a radius of 25.7 mm.

The main constraint on the longitudinal segmentation is the available space for analog cables. Currently we foresee four longitudinal readout segments per hemisphere. The two sensors closest to Z = 0 have a length of about 70 mm. The outer two sensors each have a length of about 120 mm. Each sensor is readout as a single unit. This configuration has three significant advantages. First of all, it maximizes the signal to noise ratio (S/N). The sensors closest to the interaction point have the longest analog cables, which significantly increases the capacitive load. By keeping the sensor length short the load capacitance from the sensor is minimal. Secondly, the S/N is equalized for all four readout segments. By retaining the largest segmentation possible in the central region, occupancy issues should be alleviated for the region where occupancy is highest. An added advantage is that the two lengths of sensors can be fitted on a 6" wafer. The actual length of the sensor would be determined by the wafer layout.

The total number of readout modules in the new system is limited to just 48 readouts. Since the present Run IIa detector has 912 readout modules, with a cable plant that accommodates about 940 readouts, this implies that some detectors will have to be disabled to accommodate the Layer 0 detector. This is achieved by decommissioning the H-disks.

The new silicon system will be readout with the SVX4 chip. This chip is based on the SVX3 chip, but is produced in 0.25 μm technology. This chip was designed and prototyped for the Run IIb silicon upgrade detectors. A pre-production run of 7000 chips is available. The chip has been extensively tested and meets all our specifications. The chip has been radiation tested and is shown to be very radiation hard and should easily be able to withstand the radiation doses incurred in the innermost layers. To circumvent a redesign of the entire DØ data acquisition and trigger system, the SVX4 chip will be read out in SVX2 mode. The SVX2 chip is the readout chip for the Run IIa detector and incurs deadtime on every readout cycle unlike the SVX3 chip that can run in a deadtimeless mode. The chips will be mounted on ceramic hybrids using

beryllia substrates. It is expected that the prototype hybrids for the innermost layer for the Run IIb detector can be used for the Layer 0 detector.

The digital signals will be launched onto a jumper cable from the hybrid through an AVX connector. These flex cables will be routed to junction cards located at the end of the active region on a bulkhead. There will be one junction card per two hybrids. The junction card is a passive element and simply transfers the signals from the digital cable to a twisted-pair cable. The twisted-pair cables run to the adapter cards that are mounted on the face of the calorimeter. The Layer 0 adapter card will interface to the existing data acquisition system. This adapter card has two new functions. First, it will convert 5 V lines to 2.5 V, necessary for operating the SVX4 chip. The current data acquisition system uses the SVX2 chip, in which the lines are single-ended. The SVX4 chip will be run differentially at 2.5 V. The adapter cards will convert the single-ended lines to differential lines. From the adapter card downstream, it is anticipated that we can retain the full data acquisition system as is. Some modifications may be needed for the interface boards due to the use of the SVX4 chip, but no major modifications are foreseen. It should be noted that substantial design work has been completed for the Run IIb detector and most components have been prototyped.

Some design parameters are summarized in Table 1. There are a total of 48 silicon sensors in this design, read out with 48 hybrids containing 96 SVX4 chips. The new detector will add a modest 12288 channels. The design of the Layer 0 detector is driven by the desire to keep the design simple to expedite construction. By decreasing the radius of the innermost layer from 25.7 mm to ~17 mm, the impact parameter resolution is expected to improve by a factor of 1.5. The installation of this new detector comes at the expense of the H-disks. With the addition of the Layer 0 detector we will improve on our current tracking capabilities. We will have better stand-alone silicon tracking, better impact parameter resolution and anticipate a better pattern recognition. There is no doubt that the Run IIb detector would have been a superior detector compared to the addition of a Layer 0 detector. With the addition of the Layer 0 detector we hope to recoup some of the capabilities the Run IIb detector would have offered.

	Z1	Z2	Z3	Z4
Detector length (cm)	7	7	12	12
Strip pitch (microns)	73	73	73	73
Active width (mm)	18.69	18.69	18.69	18.69
$Radius_{inner}$ (mm)	16.43	16.43	16.43	16.43
Max angle (radians)	0.52	0.52	0.52	0.52
L, effective (microns)	147.67	147.67	147.67	147.67
Analog cable length (cm)	36	34	27	20
Total capacitance (pF)	21	20.3	23.85	21.4
Total noise (electrons)	1445	1414	1573	1463
S/N (normal incidence)	15.9	16.3	14.6	15.7
S/N (edge)	7.3	7.5	6.7	7.3

Table 1 - A few Layer 0 design parameters.

3 SILICON SENSORS

3.1 Introduction

The requirements for the silicon sensors in the new Layer 0 detector are the following: the sensor has to be radiation hard, it should provide a good spatial resolution of about 15 μm, and finally the inner layer should have a large enough signal over noise to ensure a high hit efficiency. Silicon strip sensors in the inner layer constructed with about 70 μm readout pitch having intermediate strips provide precise coordinate measurement essential for good secondary vertex separation. Reliable operation of those silicon sensors in a high-radiation environment is critical to the experiment's success. Over the operating period, the inner layer of the silicon detector will be subject to a fluence of about 10^{14} 1 MeV eq. n/cm^2. In our technological design choice we were mainly guided by our experience from Run IIa detector construction as well as from the R&D work for Run IIb.

3.1.1 Lessons from Run IIa and Run IIb

Several challenges were encountered by DØ during the Run IIa silicon detector prototyping and construction. The gained Run IIa experiences and important conclusions from irradiation studies are:

- Sophisticated double-sided silicon sensors were difficult to produce and lead to lower yield and hence significant delays. Single-sided sensors however, which have been produced both by Micron for the Run IIa detector and especially by Hamamatsu for the Run IIb detector had high yields and low number of dead channels due to their relative simplicity.
- Our radiation studies[5] have indicated that double-sided (and especially 90^o double-metal) silicon sensors have increased radiation sensitivity, therefore limiting the lifetime of the inner layer of the existing Run IIa detector. Single sided sensors from Hamamatsu, however, did not show any unexpected behavior after irradiation and could be well operated beyond fluences of 2×10^{14} 1 MeV eq. n/cm^2.

3.1.2 Radiation damage in silicon

The most important damage mechanism in silicon is the bulk damage due to the non-ionizing part of the energy loss, which leads to a displacement of the silicon atoms in their lattice. It causes changes in doping concentration (and, eventually, silicon type inversion), increased

[5] "Lifetime of the D0SMT detector", document available on
http://d0server1.fnal.gov/projects/run2b/meetings/p5/march03/m_d0smtlifetime.pdf

leakage current, and decreased charge collection efficiency. Surface damage due to ionizing radiation results in charge trapping at the surface interfaces and leads to increased interstrip capacitance and electronics noise. A general overview of radiation damage in silicon detectors can be found in DØ Note 3803.

The change in the effective impurity or doping concentration $N_{eff} = [2\varepsilon\varepsilon_0/(ed^2)]\cdot V_{depl}$ measured as a function of the particle fluence for n-type starting material shows a decrease until the donor concentration equals the acceptor concentration or until the depletion voltage V_{depl} is almost zero, indicating *intrinsic* material. Towards higher fluences the effective concentration starts to increase again and shows a linear rise of acceptor like defects. The phenomena of changing from n-type to p-type like material has been confirmed by many experimental groups and usually the detector is said to have undergone a "type inversion" from n-type to p-type. The change of the effective doping concentration can be parameterized as

$$N_{eff}(\Phi) = N_{D,0} \cdot \exp(-c_D\Phi) - g_c\Phi$$

where the first term describes donor removal from the starting donor concentration $N_{D,0}$ and g_c indicates the rate of the radiation induced acceptor state increase. Hence donor removal happens exponentially whereas acceptor states are created linearly with fluence. Type inversion for standard n-type material with resistivity $\rho \approx 5k\Omega cm$ typically occurs at a fluence of about $(1 \text{ to } 2)\times 10^{13} cm^{-2}$.

The radiation-induced changes of the doping concentration are initially not stable and exhibit two main components with different time behaviors and temperature dependences. With time constants in the range of a few days a decrease in the radiation induced changes occurs soon after irradiation. This effect is called short-term annealing or beneficial annealing, because it mitigates the acceptor creation and hence the type inversion process. However, at room temperature an increase in the acceptor states appears after about two weeks of annealing leading to even higher depletion voltages. This long term or reverse annealing is a major concern because of its limiting factor for long-term operation of silicon detectors in high fluence regions. Reverse annealing can be almost completely suppressed by cooling the detector to 0^oC or less and by minimizing the maintenance periods of the silicon detectors at room temperature.

Control of leakage current is important for the operation of detectors in two aspects, one is the resulting higher shot noise, the other is the increased bulk heat production in silicon which may lead to a thermal runaway if the silicon detector is not properly cooled. The leakage current of silicon detectors increases with radiation dose due to the creation of additional gap states which will lead to more electron-hole pair generation and thus to an increase in bulk or generation current. This generation current is by far the dominant part of the entire leakage current after the silicon has been irradiated. The increase in leakage current can be parameterized as:

$$I = I_0 + \alpha\cdot\Phi\cdot A\cdot d$$

Where I_0 is the bias current before radiation, α is a damage rate coefficient usually defined at T = 20°C and dependent on particle type, Φ is the particle fluence given in particles per cm^2, A is the detector area, and d is the thickness of the detector. The exact value of α depends on particle type and energy and varies between $(2 \text{ to } 3) \times 10^{-17}$ A/cm once the silicon is completely annealed

and α reaches a constant value. The leakage current rises linearly with fluence and does not depend on either the silicon detector properties or special process characteristics during the silicon sensor manufacturing. The leakage current in silicon sensors due to generation of electron-hole pairs is strongly temperature dependent and the ratio of currents at two temperatures T_1 and T_2 is given by

$$I_2(T_2) / I_1(T_1) = (T_2/T_1)^2 \cdot \exp(-[E_g(T_1-T_2)]/[2\kappa_b T_1 \cdot T_2])$$

With κ_b being the Boltzmann constant ($\kappa_b = 8.6\times10^{-5}$ *e*V/K) and E_g the gap energy in silicon (E_g = 1.2 *e*V).

A third effect from radiation is the reduced charge collection efficiency. The primary mechanism leading to a decrease in the collection of electrons or holes is charge trapping at defect sites, *i.e.* a decrease of the carrier lifetime with increasing fluence. In addition surface damage in the silicon oxide due to ionizing radiation results in the creation of fixed positive charge at the surface boundary between silicon and silicon oxide. This leads to increased interstrip capacitances and, therefore, higher electronic noise.

Seriously damaged detectors will require high bias voltages to operate efficiently. The deteriorated charge collection can be efficiently recovered by applying a bias exceeding the depletion voltage. This overbiasing also reduces to normal values the increased interstrip capacitance due to the surface charge accumulation. High voltage operation is therefore crucial for radiation hard silicon and the breakdown voltage of the device will determine the limits of survivability.

3.1.3 Radiation hard silicon sensor designs

The CMS collaboration designed single-sided 300 μm thick n-type sensors, which were reliably working after heavy irradiation at bias voltages up to 500 V[6]. The main features of the design are p+ strips in n-bulk silicon, which are biased with polysilicon resistors and are AC coupled to the readout electronics. The front side of the detector (with p+ strips) has a peripheral n+ implantation (n-well) at the edge and is followed by a p+ single guard ring structure to prevent junction breakdowns. This guard ring design has been optimized in cooperation with Hamamatsu and is also successfully implemented with other producers. It is proven to be radiation hard and CDF is using this type of sensors for the L00 of SVX in Run IIa. Other radiation hard designs reduce the risk of an early breakdown at the edges of the silicon by including a multi-guard ring structure[7].

We note here that in the case of AC-coupled double-sided sensors (as presently used by CDF and DØ in Run IIa) the high bias voltage is applied across the coupling capacitor on one of the sides

[6] S. Braibant et al., Investigation of design parameters for radiation hard silicon, Nucl.Instr.Meth **A485**:343-361,2002.
[7] A. Bischoff et al., Breakdown protection and long term stabilization for Si-detectors, Nucl. Instr. & Meths. **A326** (1993)27-37.

(unless the electronics is floating at the same potential). Together with considerably higher costs related to the double-sided wafer processing, the requirement that AC capacitors hold off the bias voltage is a strong limitation for the double-sided detectors and we are not considering using them for the upgrade.

Another option to improve the radiation hardness at moderate fluences is the use of low-resistivity silicon as an initial detector material[8]. Low bulk resistivity of silicon corresponds to high depletion voltage of the device. For example, a 300 μm thick detector with bulk resistivity of $\rho \approx 1.0 k\Omega \cdot cm$ depletes at $V_{depl} \approx 300\,\mathrm{V}$. High initial depletion voltage values shift the type-inversion point towards higher fluences, and limits the depletion voltage growth after the type inversion, thus improving the radiation hardness of the sensor in the moderate fluence regime of up to 10^{14} 1 MeV eq. n/cm^2.

We received 13 prototype sensors from Hamamatsu for the Run IIb inner layers during the year 2002. Those sensors had been designed with single guard ring and n-well periphery. Three of them were irradiated at the KSU irradiation facility and their performance after an exposure to 10 MeV protons carefully evaluated. The results of the detailed characterization process on the unirradiated and irradiated sensors can be found in Section 3.4.

3.2 Silicon Sensors for the New Layer 0 of DØ

Based on our experience with prototype single-sided Hamamatsu silicon sensors fabricated for the terminated Run IIb detector, we propose for the construction of the new inner layer the use of AC-coupled, single-sided single-metal p^+ on n-bulk silicon devices with integrated polysilicon resistors as the baseline sensors. We have proven that bias resistors based on polysilicon are capable of sustaining the high radiation level the inner layer detector will experience. A single guard ring structure with a peripheral n-well at the scribing edge (see Figure 3), developed in cooperation with Hamamatsu's design engineers, is necessary to allow operation at high bias voltages.

[8] RD20 collaboration, "Radiation damage studies of field plate and p-stop n-side silicon microstrip detectors", Nucl. Instr. & Meths. **A362** (1995) 297-314, 1995.

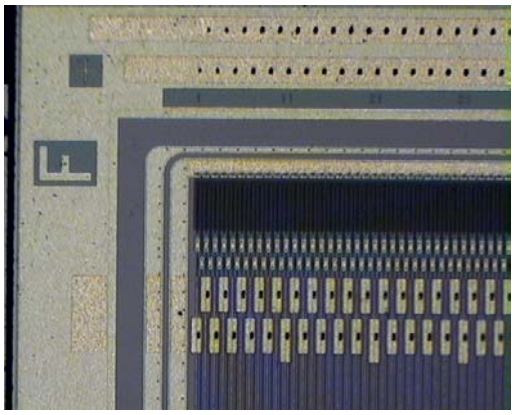

Figure 3 - Photograph of a corner of a Hamamatsu sensor with a single guard ring structure and a peripheral n-well.

We also prefer Hamamatsu as a silicon microstrip vendor since the company is capable of producing multilayered dielectric substrates for the coupling capacitors. Firstly, this will significantly reduce the number of pinholes and therefore shorted capacitors in the detector. Secondly, by using silicon nitride (Si_3N_4) in addition to silicon oxide, the coupling capacitor value can be increased while leaving the thickness of the dielectric substrate constant.

We envision using 2 sensor types for the inner layer. The geometric parameters are summarized in Table 2.

Sensor type	Active Length (mm)	Active Width (mm)	Strip pitch /readout pitch (μm)	# readout channels	# of sensors + spares
I	70 to 75	~18	~35/70	256	24 + 24
II	120	~18	~35/70	256	24 + 24

Table 2 - Geometric parameters of silicon sensors.

Specifications:	**Layer 0**
Wafer thickness	320±20 μm, wafer warp less than ±50 μm
Depletion voltage FDV	60<Udep<300V
Leakage current	< 30 nA/cm^2 at RT and FDV +20 V, total current < 1 μA at 700 V
Junction breakdown	>700 V
Implant width	7 μm
Al width	2 to 3 μm overhanging metal
Coupling capacitance	>10 pF/cm
Coupling capacitor breakdown	>100 V
Total capacitance	<1.2 pF/cm
Polysilicon bias resistor	0.8±0.3 MΩ
Defective strips	<1%

Table 3 - The main specifications for layer 0 sensors.

We plan to use intermediate strips in all sensors to improve the single hit resolution. A Hamamatsu-style single guard-ring structure is necessary to ensure high breakdown voltage after irradiation. The two aforementioned structures occupy roughly a 1-mm wide area on each edge of a silicon sensor. The main parameters of the silicon sensors are given in Table 2 and Table 3.

3.3 Fluence Estimation for Run II

Several fluence predictions for Run II have been given by Matthews *et al*[9], Frautschi *et al*.[10] and Ellison *et al*.[11] Leakage current measurements performed on the CDF SVX and SVX' silicon detectors as a function of sensor radius from the beam and delivered luminosity during the Run

[9] John A. J. Matthews et al., CDF Notes 3408 and 3937.
[10] M. Frautschi, CDF Note 2368.
[11] J. Ellison and A. Heinson, "Effects of Radiation Damage on the DØ Silicon Tracker", DØ Note 2679 (July 1995).

Ia+b provide us with a solid basis for expectations. The derived charged particle fluence quantities vary among the various authors between 1.5×10^{13} MIPs/cm^2/fb^{-1} and 1.9×10^{13} MIPs/cm^2/fb^{-1} for the new SVXII layer 0 detectors which are located at a radial distance of R ≈ 2.42 cm from the beam axis. All of the above mentioned CDF expectations have in common that the radial scaling of the fluence occurs as $R^{-1.68}$, a fact, which has been verified by independent dose measurements in the CDF detector.

To normalize the observed CDF leakage current measurements to a standard neutron or proton fluence, assumptions about the radiation damage rate constant α have to be made. Matthews[12] has given an equivalent 1 MeV neutron fluence per fb^{-1} of $(2.19\pm0.63)\times10^{13}\cdot R[cm]^{-1.68}[cm^{-2}/fb^{-1}]$. In his fluence determination, he assumed a frequently used α value for 1 MeV neutrons in order to convert the observed current increase to an effective 1 MeV neutron fluence. He took α to be $(2.86\pm0.18)\times10^{-17}$ A/cm, which is still a good value for neutrons[13] if most of the annealing of the leakage currents has occurred. Since the CDF strip measurements are not done in a fully annealed state, he applied a factor of 1.1 to α according to common annealing parameterizations[14] in order to take the partial annealing of the detector currents into account. Matthews propagated the uncertainties on silicon temperature, leakage current measurements, and α value into a final fluence uncertainty of ±30%.

The number of secondary particles produced in the Be beam tubes of the CDF and DØ experiment should be rather similar. The primary difference may be in the number of curling particles that are traversing the silicon layers more than once (caused by different magnetic field strengths in each experiment). CDF has a solenoid with 1.4 T while DØ has a 2 T field for their magnet. In a study by Ellison *et al.*[11], it was found that 50% of the total fluence will come from looper particles in the DØ magnetic field. Frautschi, who has done similar studies for CDF assumed only a 30% contribution.

The strategy of the predictions for the leakage current rise and depletion voltage changes for Run IIb presented here will be as follows: For the leakage current estimations we are using the measured strip current numbers by CDF in Run I and scale to the appropriate DØ geometries and temperatures. This approach is essentially independent of the α value, but assumes the same fluences of charged particles in the CDF and DØ experiments. In order to estimate the upper uncertainties for the leakage currents, we varied the temperature at which the CDF strip leakage current measurements took place according to their given uncertainties. Furthermore, we then increased the CDF strip currents and hence the fluence by another 20% in order to take into account a possible difference in the numbers of looper particles between DØ and CDF. More details on this approach and on the results can be found in DØ Note 3959.

The proposed 1 MeV equivalent fluence of $(2.19\pm0.63)\times10^{13}\cdot R[cm]^{-1.68}[cm^{-2}/fb^{-1}]$ by Matthews can be translated into an equivalent fluence of any other particle at any kinetic energy by knowing the corresponding so-called non-ionizing energy loss (NIEL) damage or displacement damage cross section value of the particle at a given energy. These NIEL values for neutrons,

[12] J. Matthew et al., CDF Notes 3408 and 3937.
[13] M. Moll, private communication.
[14] R. Wunstorf, Ph.D. Thesis, Hamburg, 1992.

protons, pions and electrons are normalized to the standard displacement damage cross section for 1 MeV neutrons according to an ASTM standard and are tabulated in a useful online compilation[15].

For the depletion voltage predictions, the 1 MeV neutron fluence number as given by Matthews is taken, and under the assumption of the NIEL hypothesis, we calculate the depletion voltage changes according to the latest parameters of the Hamburg model, which gives the best current phenomenological description of the change in effective doping concentration in silicon during hadron irradiation. To obtain an upper bound on the depletion voltage after irradiation, a safety factor of 1.5 is included and the 1 MeV equivalent fluence is varied accordingly.

In case of the new layer 0 sensors, the fluence estimations for Run II are therefore as follows: The new layer 0 sensors at minimum radial distances of 1.6 cm and 1.7 cm are subject to a 1 MeV equivalent fluence of 1.5×10^{13} 1 MeV eq. n/cm^2/fb^{-1} and 1.35×10^{13} 1 MeV eq. n/cm^2/fb^{-1} respectively. This numbers include the previously mentioned safety factor of 1.5.

3.4 Characterization of Prototype Run IIb Silicon Sensors

3.4.1 Available Run IIb prototypes

We have thoroughly tested 13 L1 Run IIb sensors and accompanying test structures, which were received from Hamamatsu in September 2002. The detailed results of the characterization program on the unirradiated sensor and their test structures can be found in the document "Characteristics of the Layer 1 Silicon Sensors for the Run IIb Silicon Detector"[16]. This document was prepared for the Run IIb inner layer Production Readiness Review in August 2003. The main results of the testing are summarized in Table 4.

Serial No.	Tested at	IV-Scan I(nA) @ 350V	CV-Scan FDV (V)	DC-scan strip #	AC-scan strip #	Comment	HPK Strip#	HPK I(nA) @350V	HPK FDV (V)
1	FNAL	81	110	0	0			56	130
3	FNAL	67	120	0	0			56	150

[15] A. Vasilescu and G. Lindstrom, Displacement damage in silicon, online compilation, http://sesam.desy.de/gunnar/Si-dfuncs.html

[16] The document is available at http://www.physik.unizh.ch/~lehnerf/dzero/prr/prr_l1.html

4	FNAL	54	110	0	0			69	140
6	KSU	56	130	0	13,47,267	Broken	267	76	150
7	FNAL	482	125	0	320		320	228	150
9	FNAL	174	105	0	0			55	130
11	KSU	24	125	0	0	Irradiated		55	140
12	KSU	28	115	0	0	Irradiated		65	130
13	KSU	28	120	0	0			55	140
20	KSU	31	126	0	47/48	irradiated	47/48	67	140
21	FNAL	54	120	0	0			69	140
22	FNAL	51	130	0	0			65	150
24	FNAL	67	120	0	0			85	140

Table 4 - Summary of probing results for the 13 Run IIb layer 1 silicon sensors from Hamamatsu.

3.4.2 Leakage currents and depletion voltage

All sensors that were tested up to 800 V had excellent detector leakage currents of less than 5 nA/cm^2, except one. This particular sensor had an anomalous rise in leakage current towards higher bias voltage, but still met our leakage current specifications. The difference between the total detector leakage current as measured at Hamamatsu and our test sites showed that, within the uncertainty of the measurement and taking different probing conditions such as temperatures into account, we could reproduce and verify the Hamamatsu measurements. The breakdown voltage was well above the specified 700 V for all sensors. The sensors exhibited a flat current behavior up to 800 V. A long-term test facility available at Fermilab was set up to monitor sensor behavior under bias for extended periods. No long-term drifts of the leakage currents have been observed and the sensors turned out to exhibit a rather stable bias behavior.

The depletion voltage on the sensors was determined by us to be between 105 V and 130 V using a standard CV-method. The depletion voltage on those sensors as given by the vendor was consistently higher by about 20 V, which was traced back to differences in the definition of depletion voltage.

3.4.3 Individual strip scans

The integrity of each strip was verified with AC- and DC-scans. As a result of our probing we could verify that ten sensors claimed by Hamamatsu as being flawless, do not have any open, short or pinhole. The three AC defects that were reported by the vendor for the three remaining sensors were all identified during our probing.

Nevertheless, we also found two more pinholes on sensor 6 as seen in Table 4. Unfortunately these two defects could not be confirmed since the sensor was irreparably damaged during the initial probing.

3.4.4 Other electrical properties

We have carried out numerous measurements on the polysilicon and interstrip resistances on both sensors and individual test structures. All those measurement results met well our specifications. The interstrip capacitance was measured extensively on a few sensors and on test structures. The value for the interstrip capacitance is 0.39 pF/cm to a single neighbor and 0.71 pF/cm to both neighbors. Those obtained values are again well within the specifications. The total capacitance including the backplane contribution was 1.1 pF/cm. Finally, we tested coupling capacitor values and capacitor breakdown on sensors and test structures. All that was found to be within the specifications.

3.4.5 Mechanical measurements

The first ten Hamamatsu sensors from the September 2002 delivery were measured on an Optical Gage Products (OGP) coordinate measuring machine to verify the mechanical dimensions of the sensors. The flatness of the sensors was measured by defining a grid of 11×11 points in X and Y and measuring the Z position of the top surface of the sensor. The average of the 'highest' and 'lowest' point on a sensor was 45 μm, with the highest difference of 48 μm. Our specifications called for a sensor warp of less than 50 μm, agreed to by Hamamatsu only on a best effort basis. Although it was on a best effort basis, all sensors met the specification. Combining the measurements in X and Y, gives an average cut width of the sensors of 24.312 mm and an average cut length of 79.404 mm, to be compared to the nominal values of 24.312 mm and 79.400 mm, respectively. The angle between the lines fitted to the cut edges averages 90.00 ± 0.004 degrees. All in all, the sensors are superior in all mechanical aspects, including the sensor warp.

3.4.6 Summary of Run IIb prototype sensor probing

The results of the electrical and mechanical characterizations of the Hamamatsu Run IIb silicon sensors indicate that the overall sensor quality is excellent. The sensors have low leakage

currents; they can safely be biased up to 800 V without junction breakdown and show a stable current behavior over a long-term bias test. The values for the resistors and coupling capacitors, as well as the strip capacitances are well within specifications. Moreover, the number of defective channels is very small. In all electrical and mechanical aspects, those sensors behave very well and conform to our specifications.

3.5 Silicon Sensor Performance Extrapolations for Run II

3.5.1 Leakage current and shot noise estimations

Strip leakage current measurements from CDF as a function of sensor radius from the beam and delivered luminosity are used to derive an average increase in the strip currents at T = (24±2)° C which can be scaled from their strip geometry to the DØ layer 0 configuration as shown in Table 5. In our calculation, we have taken the longer sensor, which has an active length of about 12 cm. Any other length can easily be obtained by scaling. We also estimate the leakage currents at two different radial positions, which are supposed to be the minimal distance to the beam axis for the two sublayers. The thickness of the silicon sensors is taken to be 320 μm. Radial scaling is taken to be $R^{-1.7}$.

The strip leakage currents in nA and per fb^{-1} for the new inner layer of the DØ detector at four different operating temperatures, are given in Table 6. Note that not only a readout strip, which is AC coupled to the preamplifier, but also an intermediate strip produces the same current. Therefore we do not distinguish between the two types of strips if only strip currents are considered. The calculations assume that the silicon sensors generating the leakage currents are held uniformly at the considered temperature. In reality however, the silicon sensors have temperature drops along the silicon length and an attempt to include the temperature gradient along the silicon sensors is given in the next section.

Sensor	Min. radius (mm)	Max active Length (mm)	Pitch (μm)	Strip Volume (mm^3)
1	16	120	35	1.34
2	18	120	35	1.34

Table 5 - Sensor parameters used to extrapolate leakage current and depletion voltage measurements.

Finally, the shot noise that is caused by the strip leakage currents is obtained in the following way[17]: ENC_{shot} = SQRT(12·I[nA]·τ) electrons Equivalent Noise Charge (ENC) where τ is the shaping time of the amplifier in ns, which is taken to be 132 ns. The shot noise calculations assume that the intermediate strips fully couple their noise through interstrip capacitances to the two neighbor readout strips. For fine-pitch detectors the interstrip capacitance dominates the total strip capacitance. We conservatively assume that the noise of the intermediate strips is fully coupled to the readout strips and do not include the reduction of noise due to coupling to the backplane. The expected strip noise in ENC after 10 fb^{-1} is shown in Table 7, again at different temperatures.

Table 6 - Expected strip leakage currents in nA/fb^{-1}.

Sensor	T = –10°C	T = –5°C	T = 0°C	T = +5°C
1	27.9	47.5	87.5	129.7
2	23.1	39.2	72.3	107.2

Table 7 - Expected strip noise in ENC after 10 fb^{-1}.

Sensor	T = –10°C	T = –5°C	T = 0°C	T = +5°C
1	941	1226	1665	2027
2	855	1115	1513	1843

The uncertainties in the measured CDF strip currents were 10%. In addition, there is a temperature uncertainty of ±2° C. By changing the operation temperature of SVX and SVX' from T = 24° C to T = 22° C, our estimate produces higher leakage currents by 15 to 20%. In addition to the temperature uncertainty of the leakage current measurements, the value itself was increased by 20% to take into account the possibility of different charged particle fluences between DØ and CDF due to the number of curlers in the higher DØ field. Studies using DØ radiation monitors at R = 3 cm indicate that this effect is small between 1.5 and 2 Tesla.[18] The combined resulting upper leakage current values are given in the table. This approach should be conservative enough to estimate the expected leakage currents and hence the shot noise levels in a safe way.

[17] H. Spieler, IEEE Trans. Nucl. Sci. NS-32, 419 (1985)
[18] Naeem Ahmed, private communication of "Looper Studies" in progress, August 23 2002.

3.5.2 Depletion voltage predictions

As previously mentioned, the depletion voltage predictions we are presenting are based on the 1 MeV equivalent fluence assumptions for Run II by Matthews *et al*. In addition we apply a safety factor of 1.5 to that fluence. The latest parameters for the stable damage constants, the beneficial annealing and the reverse annealing constants of the so-called Hamburg model have been used along with the Tevatron running scenario listed in Table 8. The obtained depletion voltage predictions are called standard depletion voltage predictions.

Table 8 - The Tevatron running scenario used for the calculation of the depletion voltage changes.

Year	Max luminosity pb^{-1}/week	Shutdown (months)	Max luminosity fb^{-1}/year	Cumulated luminosity fb^{-1}
2006	30	3	0.89	0.89
2007	50	4	1.53	2.42
2008	55	1	2.37	4.79
2009	55	1	2.42	7.21

.

In the standard predictions, it is assumed that the silicon detector is kept cold entirely during the luminosity runs as well as during the shutdown periods. This operation temperature is assumed to be uniform. The resulting standard depletion voltage for different operating temperatures for the new layer 0 at R = 1.6 cm are shown in Figure 4. This graph shows two calculations for layer 0 at uniform silicon temperatures of –5º C and +5º C with a starting depletion voltage of 120 V. The depletion voltage in the standard prediction does not exceed 175 V, if the sensors are permanently kept cold over the full time until 2009. There is only a marginal effect on the final depletion voltage if the sensors are kept at –5º C or at +5º C.

Moreover, the graph of Figure 4 gives two other depletion voltage predictions, which is based on a warm-up scenario: Four warming up periods, each lasting as long as the shutdown periods as given in the luminosity scenario are now included. We assume for the warm-up periods that the sensors are kept at room temperature during these short breaks in order to estimate the reverse annealing effects. One calculation was done keeping the sensors at T = –5º C during luminosity runs and the other one at T = 10º C. The reverse annealing now becomes important and will shift the depletion voltages to higher levels of up to 270 V. It is therefore important to avoid any warm up after the detector has been irradiated. We should point out, that for the operation of the silicon detectors in layer 0, a temperature as cold as possible is safer against reverse annealing, especially if warm periods are included in the depletion voltage scenario.

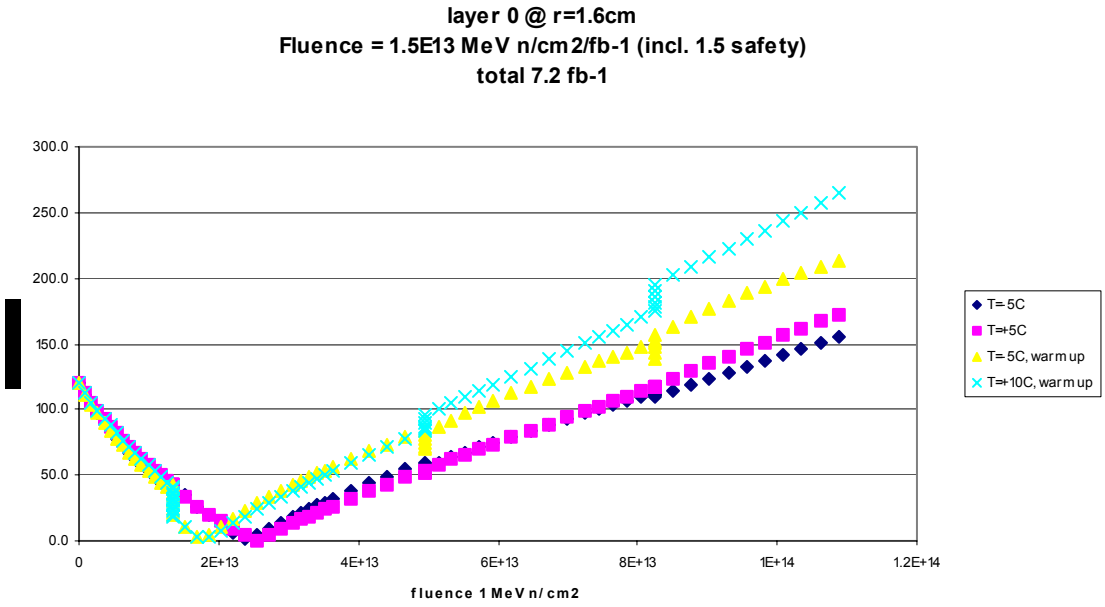

Figure 4 - Depletion voltage for layer 0 sensors as a function of fluence in Run II. The running scenario is given in table 7. The total accumulated luminosity corresponds to 7.21 fb^{-1}.

Furthermore, we should stress, that these depletion voltages represent only the voltage point at which the detector is theoretically depleted. In particular, those voltage levels do not guarantee full charge collection in the silicon. A safety margin of at least a factor of 1.5 in the bias voltage should be applied in order to have enough flexibility in overbiasing the detectors and to compensate potential charge losses due to ballistic deficits after irradiation. Since we know from our sensor characterization program on Hamamatsu prototype sensors, that they can deliver sensors with biasing capabilities of up to 700 V, we have specified the breakdown voltage of the new layer 0 sensors to be above 700 V to provide for such a safety margin.

There is some variation in the radiation damage constants and reverse annealing parameters used in the Hamburg model for different silicon wafer materials. However, these uncertainties should be absorbed in the fluence safety factor of 1.5, which we have included in the depletion voltage calculations.

We feel that it is important to point out, that we have proven that our irradiated Hamamatsu sensors withstand a dose that is at least twice the one anticipated for the inner layer of Run II. After that fluence, the sensors could be operated without breakdown risk. Those results from our recent irradiation studies are covered in section 3.6.

3.5.3 Signal to noise ratio

Signal to noise ratio (S/N) is an important parameter that ultimately limits the detector lifetime. Based on previous studies and CDF experience in Run I, S/N starts affecting b-tagging efficiency

seriously when it degrades below a value of 5 [19]. Our design goal is to keep the S/N well above 10 for all layers of the detector. In addition, we prefer to set the operation temperatures such, that the S/N of the silicon layers should not degrade by more than 15% over the course of the Run II period in order to ensure a stable and robust S/N over the full lifetime of the silicon detector.

In our signal-to-noise (S/N) estimates we assume that sensors can be fully depleted and that one MIP produces a most probable charge value of 23,000 electrons, when traversing a silicon sensor 320 μm thick. We have considered several contributions to the total noise:

- Noise in the front end due to capacitive load: the analog cable in layer 0 contributes with 0.4 pF/cm to the total capacitive load. The silicon sensors are conservatively assumed to have a total load capacitance of 1.4 pF/cm, dominated by the interstrip capacitance. The ENC noise behavior of the front end chip (SVX4) for the bandwidth of interest is taken to be 450+41*C(pF) according to the specifications.
- Noise due to the serial resistance of the aluminum traces of the silicon sensors and the copper traces of the analog cable: This noise depends on the bandwidth and total load capacitance as well. The serial noise is about 490 electrons for a 12 cm long layer 0 sensors having a 24 cm long cable.
- Shot noise from detector leakage current as calculated before. A shaping time of 132 ns is assumed
- Thermal noise due to the finite value of the bias resistor (~250 electrons).

[19] J. Albert et al. " The relationship between signal-to-noise ratio and b-tag efficiency." CDF Note #3338.

In the following, we will present the expected signal to noise ratio based on the noise input assumptions mentioned above as a function of luminosity for layer 0. We plot the S/N for different temperatures in order to derive temperature bounds for the operation of the various layers. We further limit our calculations to the most unfortunate case, which is a 12 cm long sensor ladder at a radius of 1.6 cm with a cable length of about 24 cm.

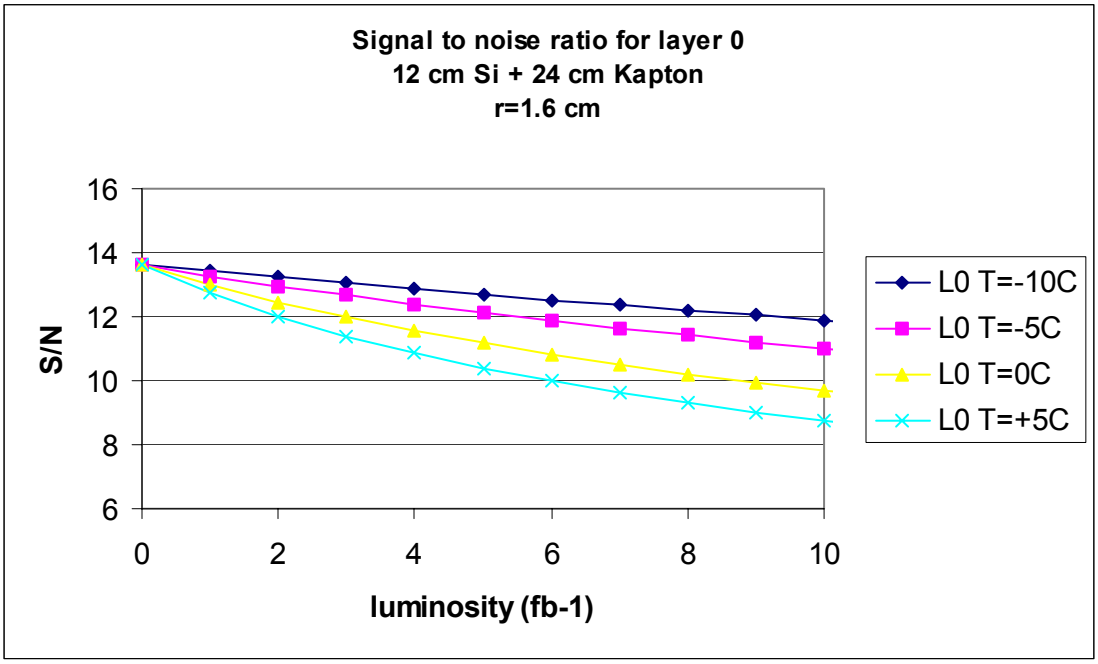

Figure 5 - Signal to noise ratio for layer 0 modules as a function of luminosity for different running temperatures.

Figure 5 shows the S/N behavior as a function of luminosity for a layer 0 module. Due to the large load capacitance of this assembly, the S/N will be initially about 14:1 in our conservative S/N estimation. A further degradation by additional shot noise is expected. Therefore, the best strategy would be to keep the detectors in the innermost layer as cold as possible. The S/N will then remain almost as large as 12 after 10 fb^{-1}, so that the S/N change can be kept at a level of 15%. It is therefore very important to provide the cooling for this layer such that silicon temperatures of approximately T = –10º C can be reached at the end of the running period. This will give additional safety margin against reverse annealing in case of warming up periods.

In summary, based on our estimations of leakage currents, depletion voltage and S/N we should intend to keep the silicon sensors at a temperature of T = –10° C.

3.6 Radiation Testing of Silicon Sensors

To check the breakdown behavior of the silicon sensors after irradiation and to compare our predictions to measured depletion voltage values, we have tested several single sided Hamamatsu silicon sensors at a Radiation Damage Facility at Kansas State University.

3.6.1 Radiation Damage Facility

The irradiation tests that are described here were carried out at the James R. Macdonald Laboratory[20] at Kansas State University. The facility provides a 7MV Tandem van de Graaf accelerator. The beam energy of the protons was set to 10 MeV. The irradiation dose was carefully measured using charge collected by a Faraday cup, which was read out by a charge integrator. An independent verification and cross check of the Faraday cup dose determination was done using activation measurements of 1.5 mil thick Cu foils confirming the Faraday cup measurements on a 15% level. The activation analysis carried out at KSU was double checked at FNAL. Exact details of the beam properties, the experimental setup, the Faraday cup calibrations and the flux cross checks by two independent activation measurement analysis are summarized in the note "Flux Normalization for 10 MeV Protons Used in Run 2b Radiation Tests"[21].

3.6.2 Run IIb detector irradiation studies

We have performed a set of irradiation studies on single sided Run IIb Hamamatsu prototype sensors detectors as well as on a set of planar test diodes. Three Hamamatsu L1 silicon sensor prototypes were irradiated in 10 MeV protons beams up to a final fluence of 9.35×10^{13} 10 MeV p/cm^2 and the irradiation on the diodes was performed at five different fluence points up to an accumulated fluence of 1.32×10^{14} 10 MeV p/cm^2. This very high fluence of low energy protons would lead to radiation damage in silicon that is at least 3 times higher than expected over the course of the Run II, if a naïve NIEL scaling is applied.

The irradiation of the L1 silicon sensors was performed in up to seven successive steps, until the total dose was accumulated, while for the diodes the irradiation of each individual diode was performed in a single dose. After each irradiation the detectors were properly annealed and the depletion voltage and leakage currents were measured. Detailed results on the electrical characterization of the sensors and diodes can be found in the document "Measurements on irradiated L1 sensor prototypes for the DØ Run IIb silicon detector project"[22].

3.6.3 Results of irradiated sensors

The measured leakage currents of the sensors and diodes after radiation exposure have strongly increased as expected due to irradiation induced bulk damage. We could confirm that the leakage current increase was directly proportional to the fluence and volume of the detectors. The measured leakage currents showed the normal temperature scaling that is expected for generation currents. For beams of 7 and 10 MeV protons we determined the current related damage constant

[20] http://www.phys.ksu.edu/area/jrm
[21] This document is available at http://www.physik.unizh.ch/~lehnerf/dzero/irradiation/dosimetry_writeup_new.pdf
[22] This document is available at http://www.physik.unizh.ch/~lehnerf/dzero/prr/prr_l1_doc/PRR_L1_irrad_v3.0.pdf

α to be 18×10^{-17} A/cm and 12×10^{-17} A/cm respectively. These results are in excellent agreement to a silicon diode irradiation study[23] that has been carried out by the ROSE collaboration on low energy proton beams. Consistent with the findings of the ROSE group, we observed about 40% less radiation damage than anticipated by naive NIEL scaling.

We did not observe any major breakdown of the irradiated L1 sensors up to 800V. The change in effective doping concentration as measured in the depletion voltage after irradiation was consistent with the standard parameters of the "Hamburg"-model[24]. Other measurements on the irradiated sensors included the characterization of the polysilicon resistors, the coupling capacitors, the strip capacitances and the detection of newly developed pinholes. While we did not observe any change in the resistor and coupling capacitor values, the total strip capacitance increased from 1.1 pF/cm to 1.5 pF/cm after receiving a total dose of 9.35×10^{13} 10 MeV p/cm^2. This increase is entirely due to increased interstrip capacitance on the sensors and should be verified again.

In summary, the irradiation study revealed that the bulk damage effects on irradiated Hamamatsu prototype sensors occurred at the expected level. There were no signs of any enhanced radiation softness or any anomalies, except for increased interstrip capacitances that were observed after the full radiation dose. The heavily irradiated sensors could be well biased and operated. It is important to note, that those sensors have received a total proton dose corresponding to a layer 0 running with an integrated luminosity of at least 15 fb^{-1}. This number takes the true reduced hardness factor of 10 MeV low energy protons into account, which deviates by 40% from theoretical NIEL scaling.

3.7 Conclusion

The revised projected integrated luminosity of Run II of up to 8 fb^{-1} will necessarily result in a particularly harsh radiation environment. Reliable operation of silicon sensors in such conditions is crucial to the experiment's success. We were guided in our design and technology choice by our experience in Run IIa and by results from our R&D for Run IIb. We will use single-sided silicon sensors from Hamamatsu and we are confident of having chosen the right sensor parameters and specifications. Our estimates, supported by the results of the irradiation tests, show that these sensors will be able to withstand the radiation dose equivalent to a luminosity of 15 fb^{-1} with a significant safety margin in layer 0.

The depletion voltage for layer 0 sensors is expected to reach about 170V for the assumed Tevatron Run II scenario of accumulating a luminosity of 7.21 fb^{-1} between 2006 and 2009, if no warm-up occurs. The layer 0 sensors will be specified to breakdown not earlier than 700 V, providing much flexibility in overbiasing these detectors. Our studies on the silicon sensor prototypes have shown, that Hamamatsu can produce such devices. The global operation temperature of the new inner layer at T = –10° C in order to keep the S/N drop to about 15% and

[23] D. Bechevet et al. "Results on irradiation tests on planar silicon detectors with 7-10 MeV protons", NIM A 479 (2002) 487

[24] M. Moll et al., "Leakage currents of hadron irradiated silicon detectors – material dependence", NIM A 426 (1999) 87

above 12. Operation temperatures above T=0° C should be avoided, since the S/N will then drop to 10 or below. Warm periods of several weeks for maintenance should be avoided in order to prevent reverse annealing.

4 MECHANICAL DESIGN, STRUCTURES, AND INFRASTRUCTURE

4.1 Overview

The existing tracker region, the present silicon, and the present 1.5" outside diameter beryllium beam tube is shown in Figure 6. Silicon is supported by separate north and south double-walled carbon fiber – epoxy support cylinders which, in turn, are supported from fiber tracker barrel 1 near Z = 0 and at approximately Z = ±830 mm. The beam tube is supported by membranes of the cylinders at approximately Z = ±830 mm. In addition, it is positioned by structures at each outermost H-disk to control transmittal of forces and moments as End Calorimeters are opened and closed.

The current tracker is aligned to the ideal Central Fiber Tracker (CFT) system. This was done by surveying the existing support cylinders within the CFT prior to installation of the CFT. Subsequently the silicon barrels and disks were precisely aligned in this coordinate system, within the north and south support cylinders, at SiDet. Finally the CFT and Silicon system, concentric to very high accuracy, form the ideal axis to which the Tevatron beam should be aligned.

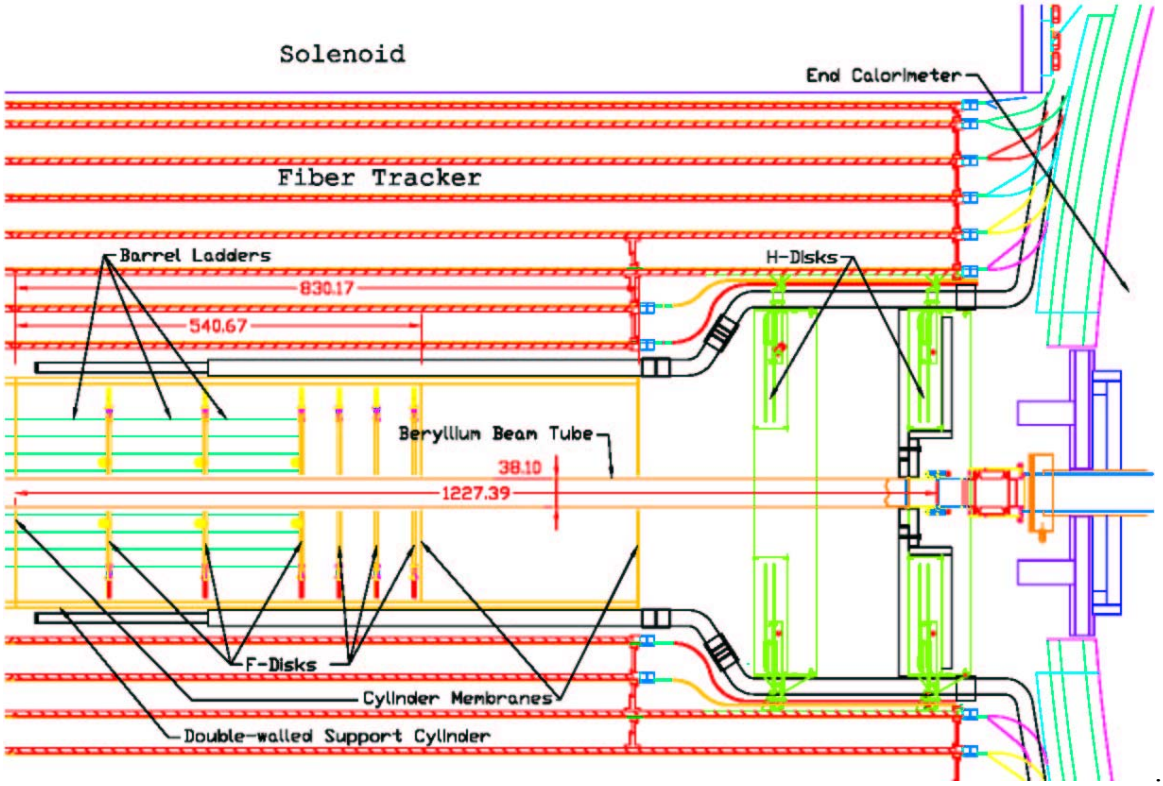

Figure 6 - A portion of the present tracker region showing ladders of three silicon barrels, six F-disks, and two H-disks.

Figure 7 shows the space available for a new Layer 0. Layer 0 is to fit between the 1.16" outside diameter beryllium beam tube and the existing silicon tracker. The active Layer 0 silicon length is expected to span Z = ±380 mm, the barrel region of the current detector. Structural support for Layer 0 is provided by the double-walled cylinder membranes near Z = ±830 mm. Our present expectation is that Layer 0 would be built as a full-length structure rather than separated into north and south halves. Then all portions of Layer 0 must clear the existing silicon and pass through openings, nominally 1.875" diameter, in support cylinder membranes near Z = 0, Z = ±540 mm, and Z = ±830 mm. Layer 0 cables follow the beam tube until they have passed through the openings in the Z = 830 mm membranes.

To remain within the constraints of the existing silicon readout system, at least one of the two H-disks at each end of the silicon will no longer be used. All H-disks may need to be removed, at least temporarily, to ease installation of Layer 0. After Layer 0 has been installed, the outermost H-disk enclosures or equivalents are needed to aid in positioning the beam tube and to provide a dry gas enclosure for the silicon region. Coolant and dry gas purge for Layer 0 will be supplied from manifold connections now used by H-disks.

We plan to consider the option of enlarging the central openings in the Z = 830 mm membranes to provide more radial space for cables and services and then adding annular cover disks to position Layer 0 and the beam tube, guide cables and service connections, and re-constitute the dry gas enclosure.

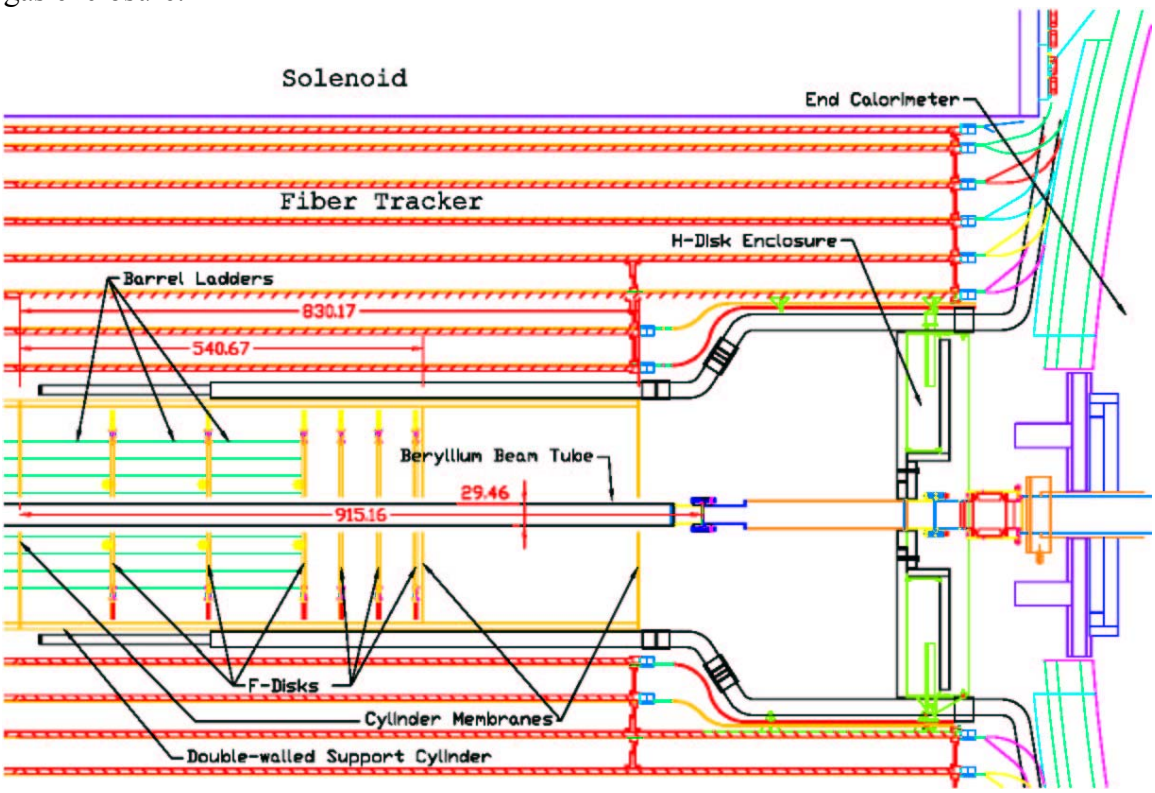

Figure 7 - The same region of the tracker with a 1.16" outside diameter beam tube and one H-disk removed.

4.2 Geometry

The basic geometry of the design is a six-fold layout with sensors at two radii, but utilizing sensors of only one width. The sensors will have 256 channels and a pitch of 70 to 75 μm. The main space constraints are imposed by requirements on radial clearance to the beam tube and to the opening in the existing silicon support structures in the installed Run IIa detector. These are described in detail below. The new Layer 0 detector, with the inner support structure and outer screen, must reside in $16.0 < R < 22.0$ mm. The available space is illustrated in Figure 8.

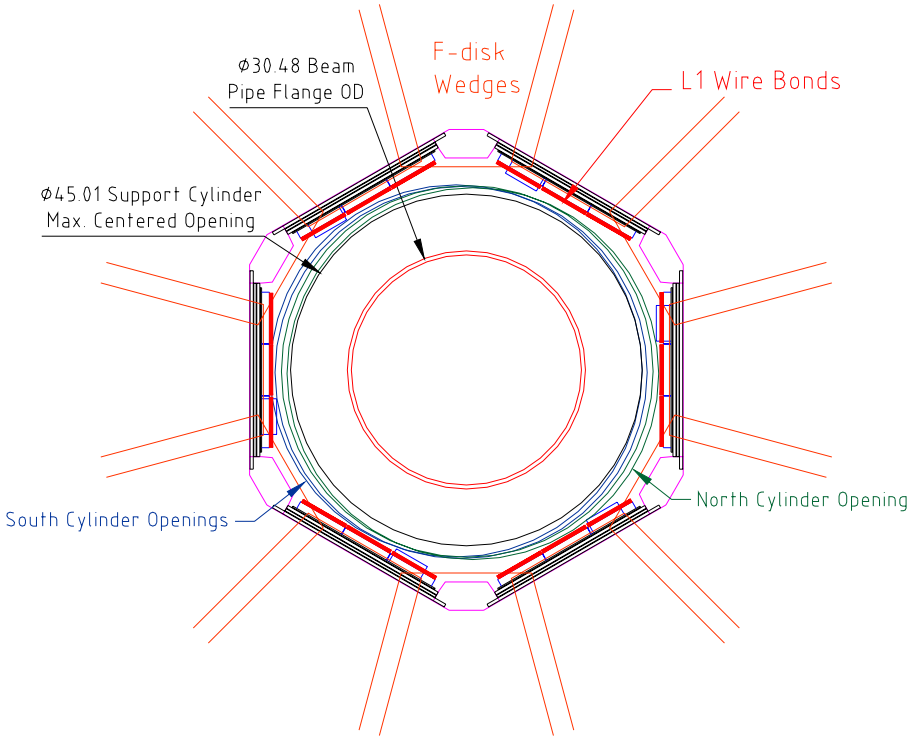

Figure 8 - Available space in the Run IIa detector using the Run IIb beam tube.

4.2.1 Space constraints

There are two areas of concern with regard to installation of a Layer 0 detector into the existing tracker. First, there are six carbon fiber annular membranes that are part of the existing silicon tracker support cylinders. The second issue is clearance to the L1 ladders and/or F-disk sensors

of the existing tracker. We have investigated the geometry of the as-built tracker and have found that the former dictates the physical limitation. This is preferable as the L1 ladders have extremely delicate wire bonds that extend inwards towards the beam axis. Fortunately the openings in the support cylinders provide some measure of both protection to the existing tracker and guidance for installation of the new Layer 0 detector.

Of the six membranes in the Run IIa support structure, we have precise survey data on the locations of four in the ideal coordinate system of the detector. Two of these four membranes are at Z = 0 and two at |Z| = 830 mm. The remaining membranes, which we do not have survey data for, sit just beyond the end F-disk assemblies at |Z| ≅ 540 mm. The nominal diameter of the central holes in these annular disks is 47.625 mm. However, the centers of these openings are not aligned to the ideal detector axis by as much as 1.3 mm. The resulting maximal circular opening centered on the ideal detector axis that inscribes the four known openings has a 45.01 mm diameter. We wish to retain a 0.5 mm radial clearance for installation and accommodate a 0.3 mm wall thickness outer screen around the new Layer 0 detector and another 0.2 mm radial clearance for installation of this outer screen. This results in a maximum allowable radius of 21.5 mm for any components in the Layer 0 sensor-hybrid modules. With an outer screen having an OD of 22.0 mm the radial clearance to the L1 ladders is 2.7 mm, assuming 0.5mm bond height above the SVX chip surfaces. The sensors sit roughly 3.5 mm outboard of the outer screen for Layer 0 so capacitive noise pickup in L1 due to the presence of Layer 0 should not be an issue. The innermost extent of the F-disk sensors is 4.0 mm beyond the outer screen radius, again providing adequate installation clearance. Capacitive noise pickup in the wedges would be insignificant in any case as they are perpendicular to the outer screen.

4.2.1.1 Beam Tube

The beryllium beam tube purchased as a spare for the existing detector and for use with the full upgrade will be used. The beryllium portion has an outside diameter of 1.16” and a wall thickness of 0.020”. Stainless steel transition pieces at each end carry knife-edge flanges for connections to the other beam tubes of the experiment. The outside diameter of the knife-edge flanges and of the transition regions from beryllium to stainless steel is 1.20”, only slightly larger than that of the main portion of the tube. The length of the beryllium portion of the beam tube is 69.06”. The overall length, from knife-edge to knife-edge, is 72.01”.

The beam tube was procured from Brush-Wellman Electrofusion. Dimensional inspections were performed at SiDet on a coordinate measuring machine. The measured deflection of the beam tube under its own weight agrees well with spreadsheet calculations (Figure 9); differences are consistent with uncertainties in the beryllium elastic modulus, the support points for the CMM measurement, and the thickness of the tube wall. Support during the measurements was at approximately Z = ±35”.

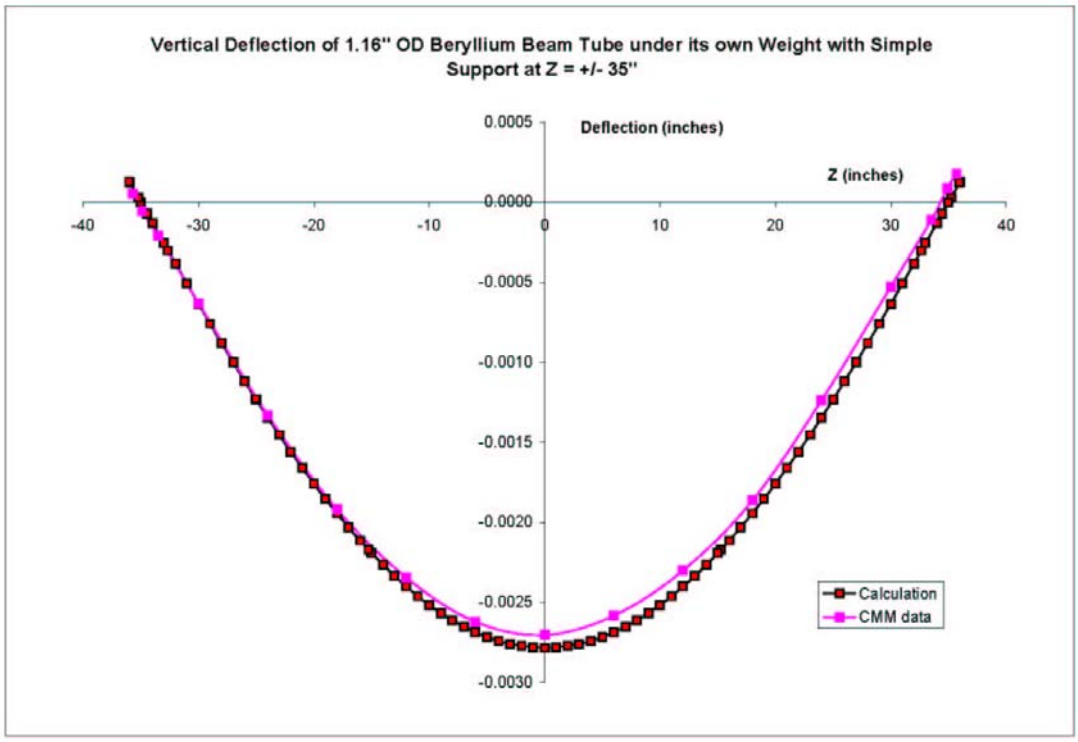

Figure 9 - Deflection of the beryllium beam tube under its own weight with simple support near Z = ±35".

Actual support of the beam tube is expected to be from the carbon fiber – epoxy end membranes of the silicon support cylinder at Z ≈ ± 32.64" (slightly different from the locations of the CMM data). The same calculation yields a beam tube deflection of 0.0023" for support at the membrane locations as shown in Figure 10.

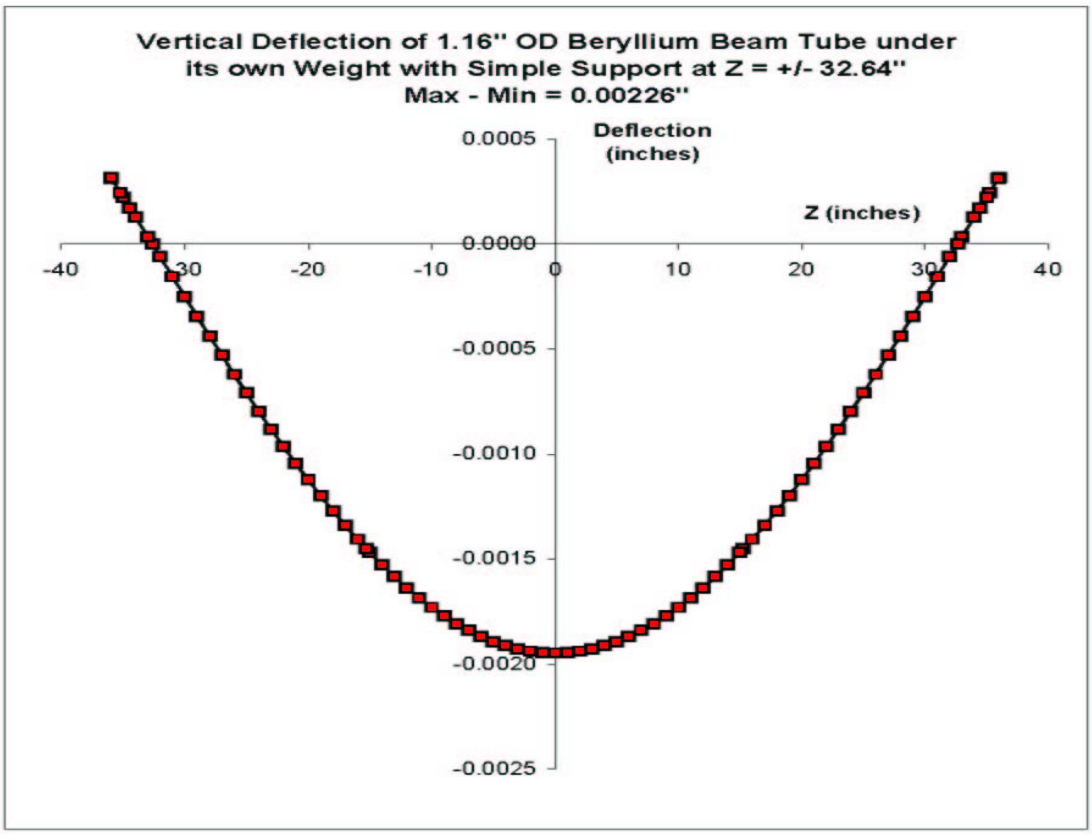

Figure 10 - Calculated deflection of the beryllium beam tube under its own weight with simple support at Z = ±32.64".

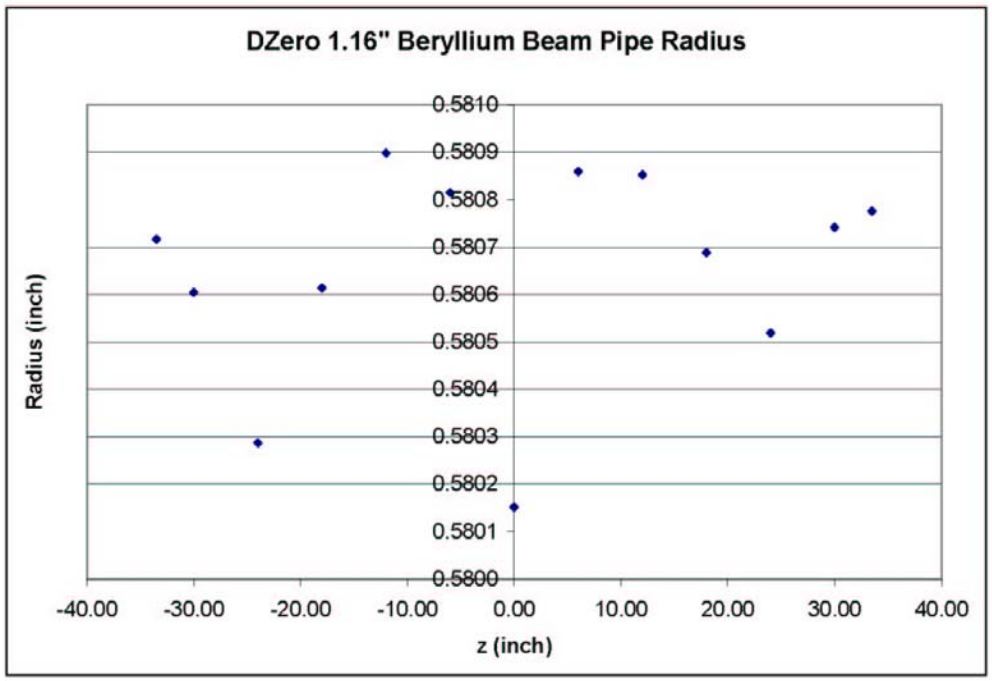

Figure 11 - Measured radius of the beryllium portion of the beam tube as a function of Z. The nominal radius is 0.580". At the worst location, the measured radius exceeds nominal by 0.0009".

Our design requires that a carbon fiber – epoxy support structure, which carries silicon, hybrids, and associated components, can slide over the beam tube. Given these small gravitational deflections and the excellent roundness of the beam tube (Figure 11), deviations of the beam tube from a straight cylinder dominate clearance requirements. Measured deviations from straightness are shown in Figure 12 and Figure 13. The dominant contribution to lack of straightness is angular misalignment in a joint between two beryllium sections at Z = -15". The effective outside diameter of a cylinder that would include all measurement points is 1.2006". That diameter is essentially the same as the 1.200" diameter of the end flanges. The beam tube can be oriented so that gravitational deflections, which are small, improve the beam tube straightness. Therefore, normal clearance to allow a carbon fiber structure to slide over the beam tube flanges should also be sufficient to ensure clearance to all other locations of the beam tube. To ensure adequate clearance, our design requires a minimum diameter of 1.207" for the carbon fiber – epoxy support structure. Clearances will be rechecked before the design is made final.

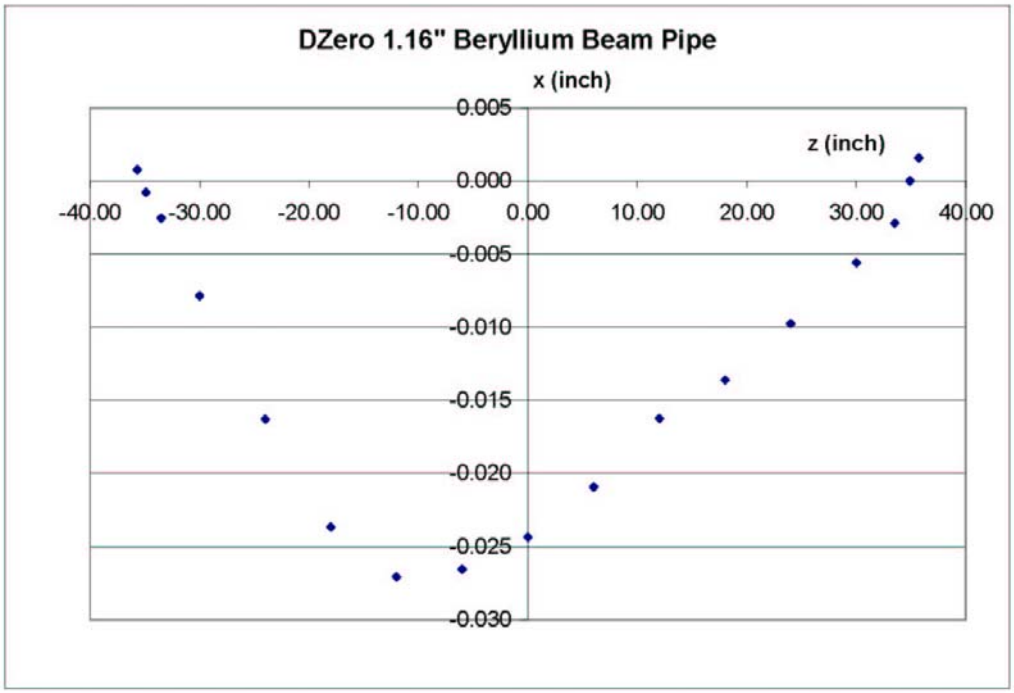

Figure 12 - Measured beam tube deviation from straightness, X coordinate.

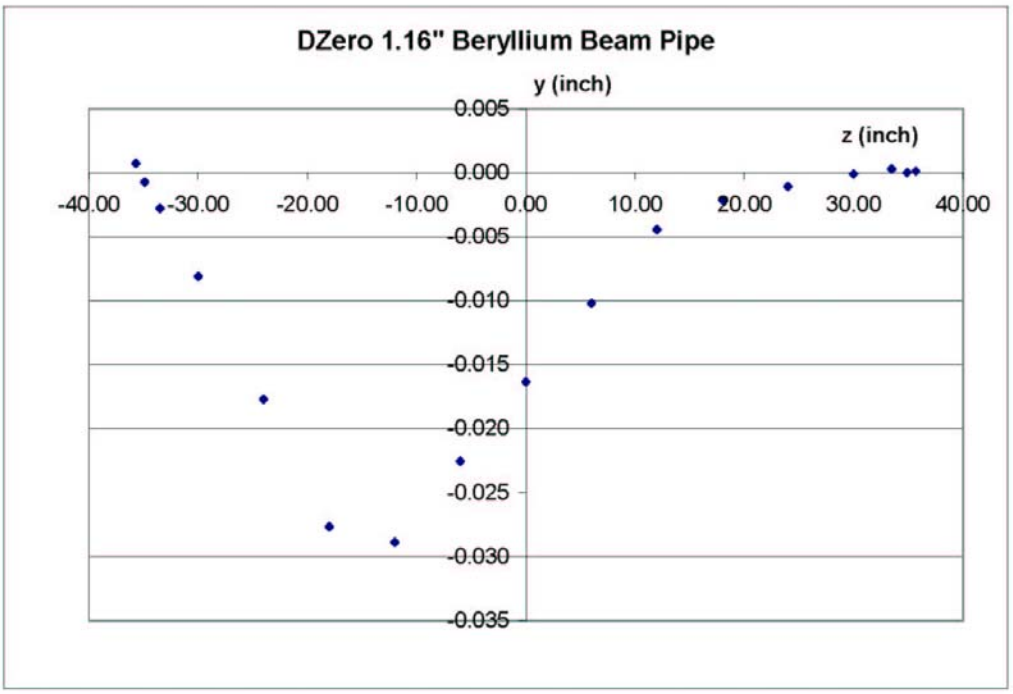

Figure 13 - Measured beam tube deviation from straightness, Y coordinate.

4.2.1.2 Openings in the existing support cylinders

The alignment of the present 1.5" beryllium beam tube with silicon support cylinder openings is shown in Figure 14, Figure 15, and Figure 16. Spacers at the Z = ±830 mm membranes position the beam tube with respect to membrane openings. Nominal F-wedge profiles are shown in orange. Nominal positions of innermost ladder silicon are shown in black with components of the onboard readout (SVX-IIe chips and capacitors) shown in blue. The 1.5" beam tube is shown in magenta and green. The four cylinder openings are not perfectly aligned. That was not a significant issue for the present silicon, but will be a greater issue for a new Layer 0. Alignment of Z = 0 openings in north and south cylinders (Figure 15) presents the greatest constraint. An inscribed circle and limiting dimensions have been included in this figure. The result is a clear diameter of 1.807" ± 0.020". We are likely to be able to reduce uncertainty in the clear diameter by re-examining measurement data, but have not had the opportunity to do that. Openings at Z = ±830 mm remain outside that clear diameter.

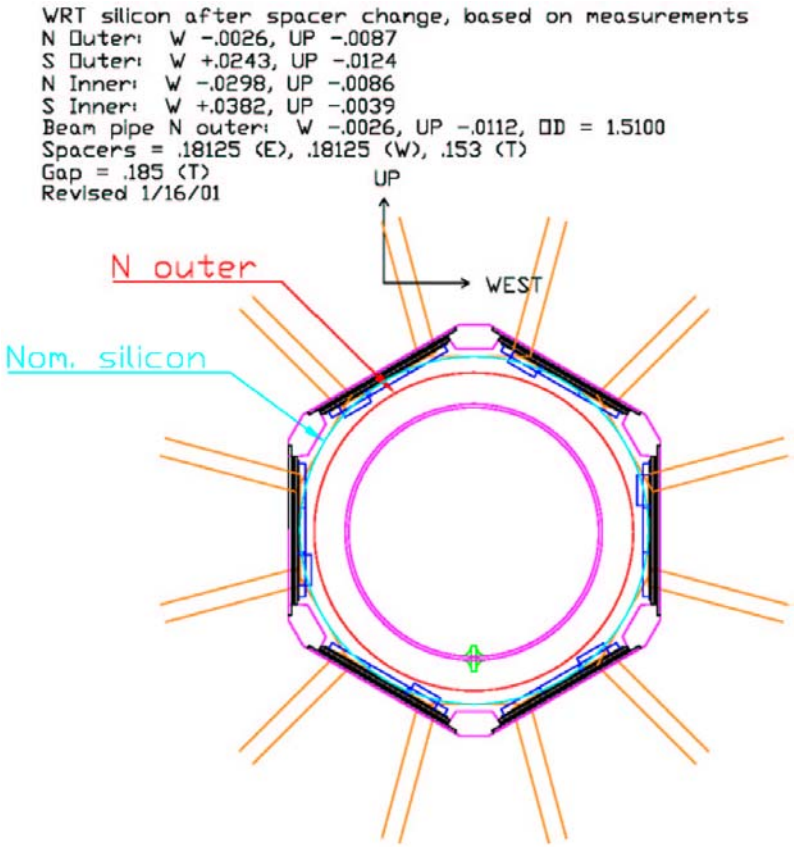

Figure 14 - Opening in the Z = 830 mm membrane of the north support cylinder.

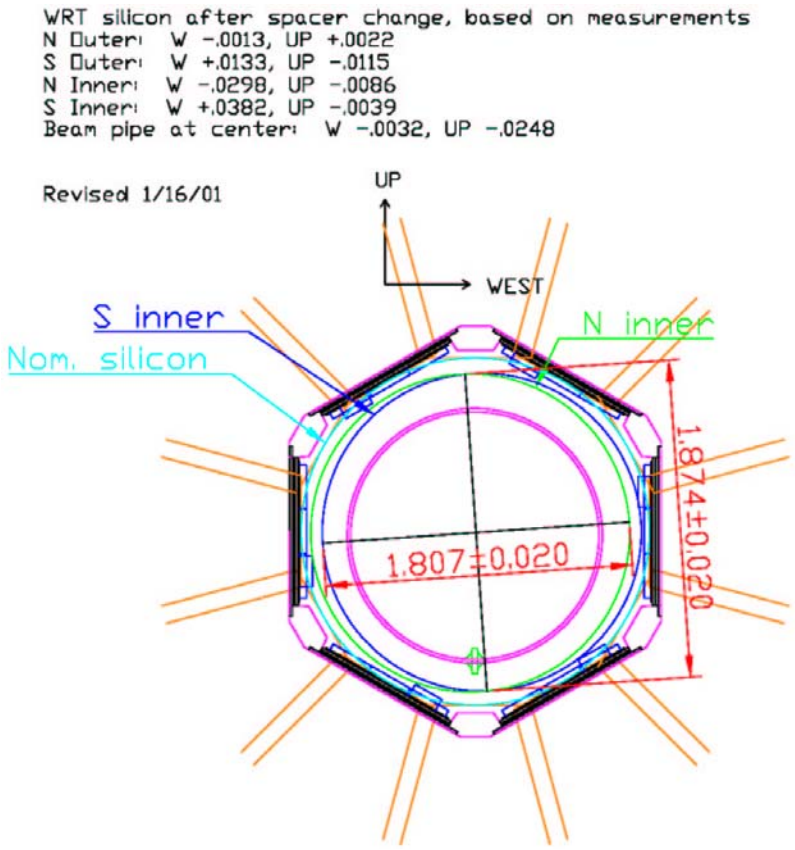

Figure 15 - Openings in the north and south support cylinder membranes near Z = 0.

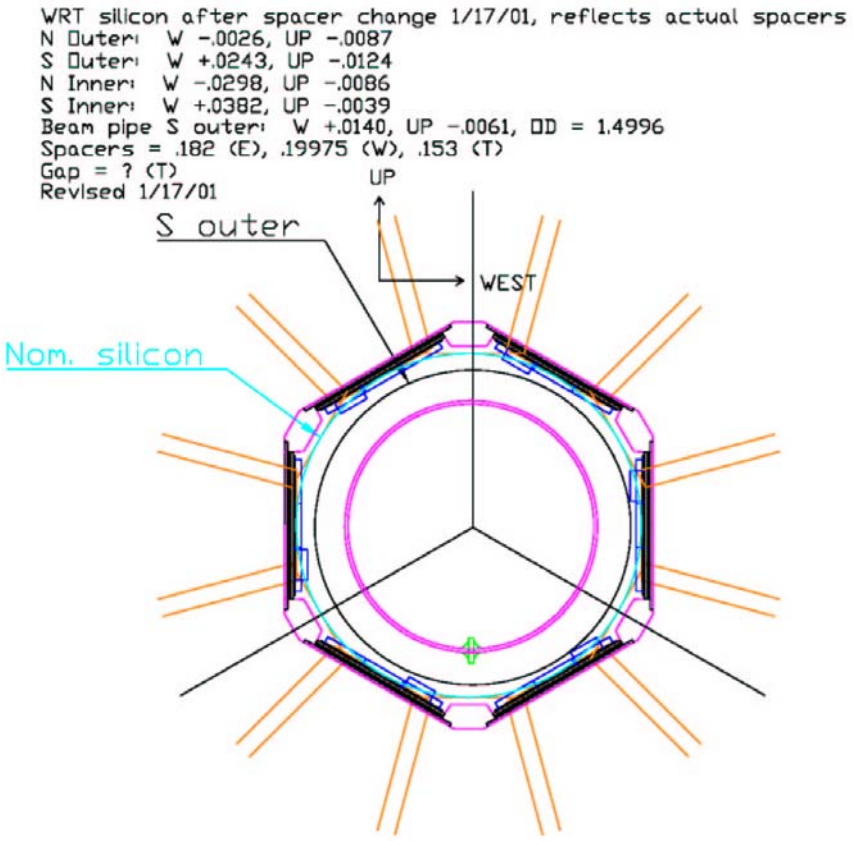

Figure 16 - Opening in the Z = 830 mm membrane of the south support cylinder.

4.2.1.3 Capacitance issues

The support structure for Layer 0 silicon and its readout relies strongly upon the use of carbon fiber – epoxy structures. Control of noise and pick-up requires that those structures share a common ground with the silicon sensors and readout hybrids. That ground should be electrically isolated from other grounds, such as that presented by the beam tube. Our goal is a capacitive reactance not less than 10 ohms at 10 MHz. Figure 17 and Figure 18 show gap between concentric cylinders versus capacitive reactance and radius of an outer cylinder versus capacitive reactance. The radius of the inner cylinder has been chosen to match the measured outside diameter of the 1.16" beryllium beam tube. Kapton insulation 0.004" has been assumed on the outer surface of the beam tube. The calculations show nearly linear behavior between gap and reactance. They provide a guide to allowable contours of the inner surfaces of the support structures. Linearity suggests that, for non-circular shapes, it is reasonable to average the gap over all phi. The required average gap is about 1 mm. The consequences of non-concentric cylinders and of non-circular shapes remain to be investigated in greater detail.

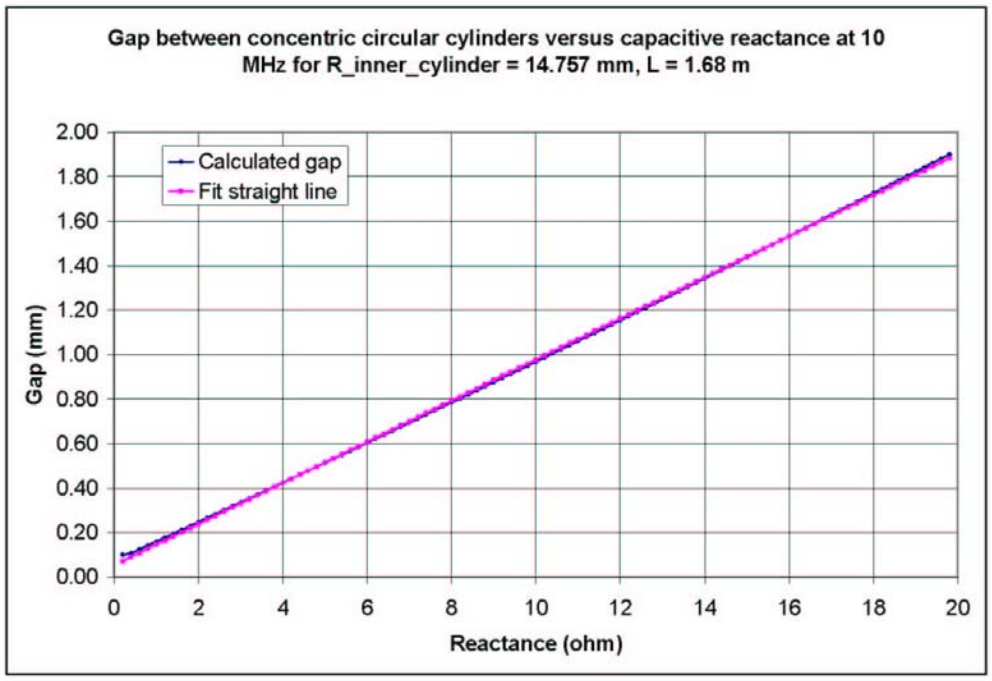

Figure 17 - Gap between concentric circular cylinders versus capacitive reactance at 10 MHz.

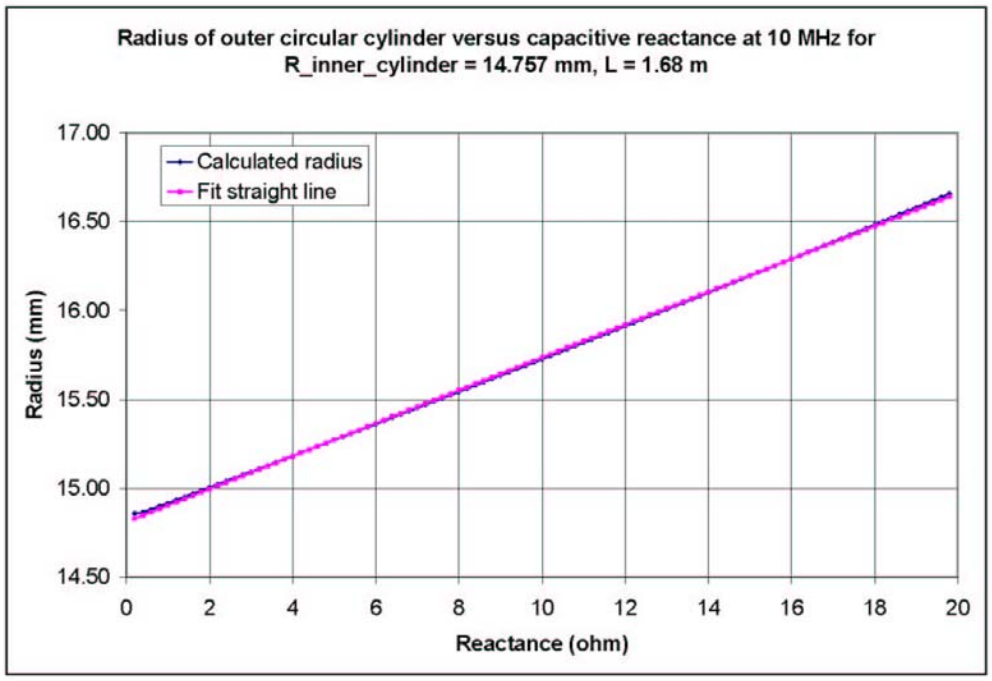

Figure 18 - Radius of an outer cylinder versus capacitive reactance at 10 MHz.

4.3 Mechanical Design and Assembly

The support structure for Layer 0 is a carbon fiber assembly consisting of inner and outer carbon fiber shells. The design presented in this document uses conservative values for thickness of materials and glue joints. We plan to continue to review all material choices with the goal of improving acceptance and ease of fabrication. This design is geometrically similar to the Run IIb L0 and L1 silicon support structures for which full prototypes have been fabricated. Heat generated by the sensors and hybrids is transferred through the carbon fiber structure to cooling tubes inserted between the inner and outer carbon fiber layers. The cooling tubes will be manufactured from Peek tubes that are formed into the desired shape. Extensive prototyping in forming Peek tubes was carried out for the Run IIb layers 2 through 5 structures. The manifolds required to combine all of the cooling circuits in one inlet and outlet connection also serve as structural bulkheads. A preliminary FEA mechanical model of the structure described in section 4.3.3 shows that the expected deflections are within acceptable limits. A description of the fabrication procedures, based on our Run IIb L0/1 experience, is presented in section 4.3.4 and section 4.3.5. Design, installation, and alignment of sensor – hybrid modules are described in section 4.3.6. Materials and radiation lengths are summarized in section 4.3.7.

4.3.1 Design in the sensor region

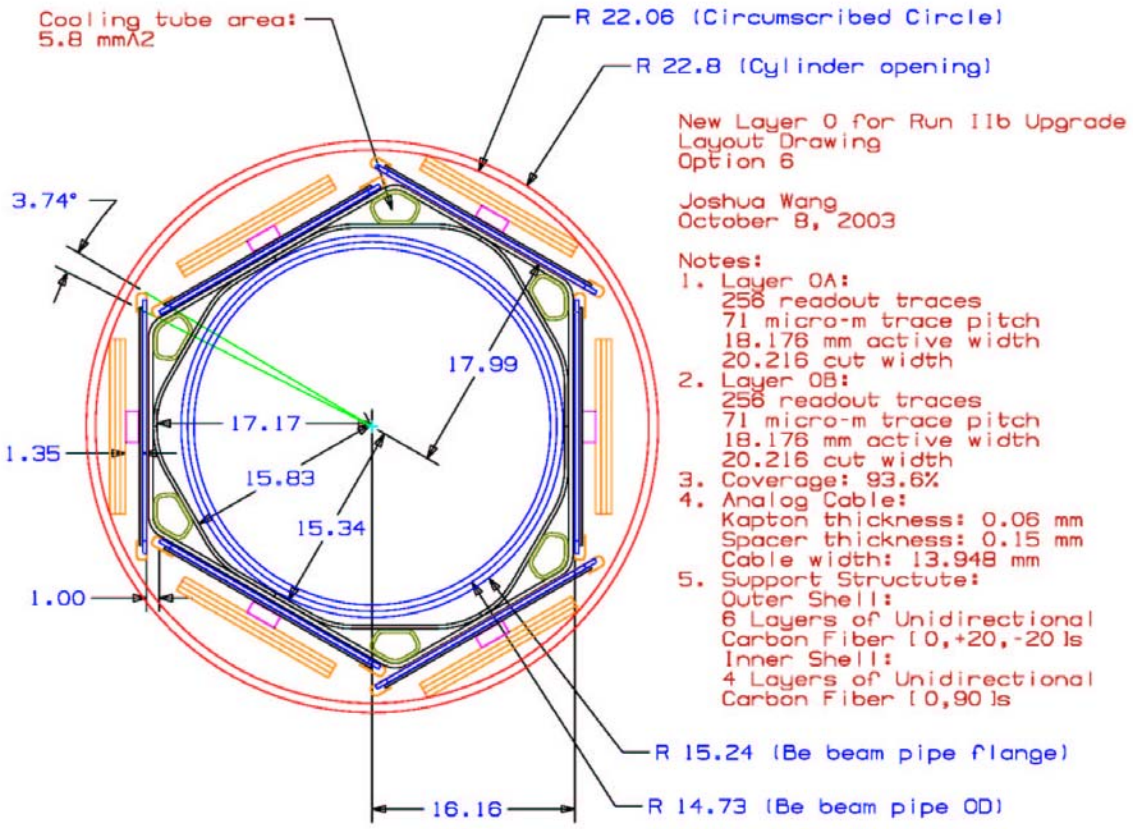

Figure 19 - Preliminary design in the sensor region

The Layer 0 sensor region is shown in Figure 19. The support structure consists of a twelve-sided inner shell and a six-sided outer shell. The inner shell has a 4-layer [0°/90°]s lay-up of K13C2U high modulus carbon fiber. The outer shell has a 6-layer [0/+20°/–20°]s lay-up of K13C2U high modulus carbon fiber. This structure extends from Z = –380 to Z = +380 mm. A 0.025 mm kapton sheet with an embedded copper mesh is co-bonded to the outer shell for grounding connections.

The silicon sensors are mounted on the outer shell using epoxy adhesive. Two insulating layers of kapton separate the silicon backplane from the grounded carbon/epoxy structure. One of the insulating kapton layers, which has copper mesh circuits with vias is co-bonded with the outer carbon fiber shell to help ground the carbon fiber to the sensors. There are two layers of sensors sitting at different radii (Layer 0A and Layer 0B). Analog cables connect each sensor with its corresponding hybrid.

4.3.2 Design in the hybrid region

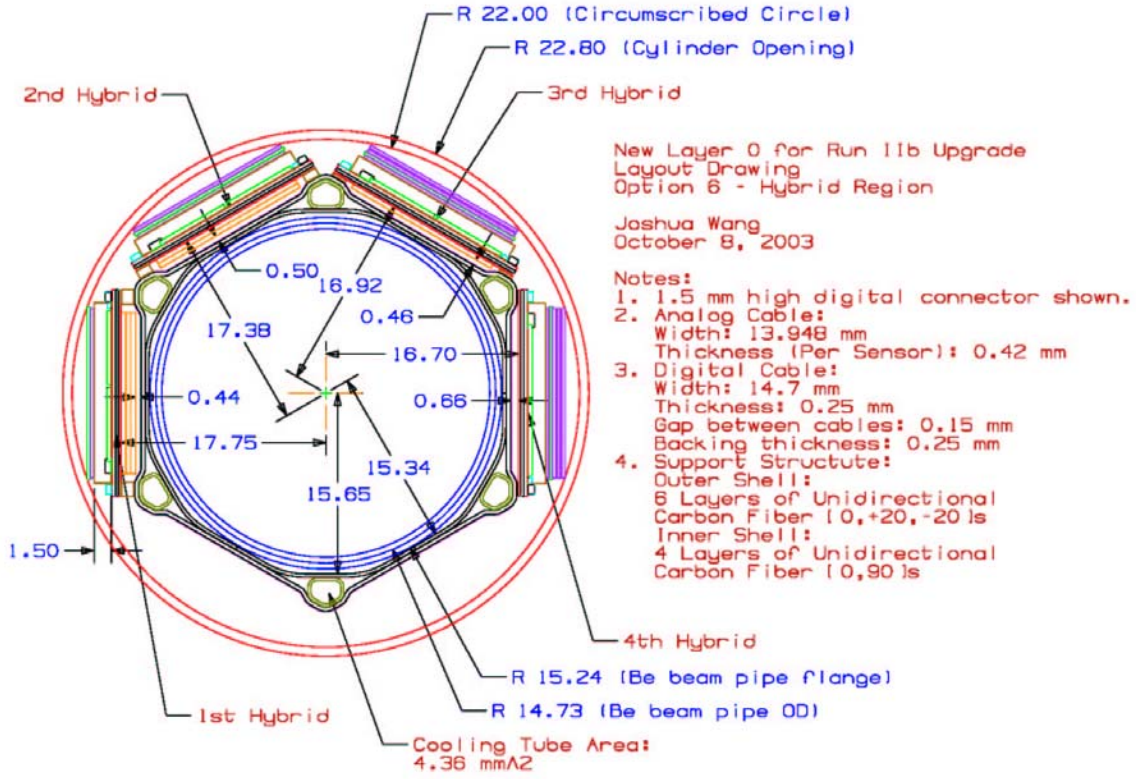

Figure 20 - Preliminary design in the hybrid region.

The Layer 0 hybrid region is shown in Figure 20. The support structure consists of a twelve-sided inner shell and a castellated outer shell. The inner shell has a 4-layer [0°/90°]s lay-up of K13C2U high modulus carbon fiber. The outer shell has a 6-layer [0/+20°/–20°]s lay-up of K13C2U high modulus carbon fiber. The outer castellated shell extends from Z = ±400 mm to Z = ±580 mm, the length of 4 hybrids (35 mm) and 10 mm gap between each hybrids. The inner shell extends from Z = ±400 mm to Z = ±830 mm and the thickness can be doubled after the hybrid support region to increase the stiffness of the structure.

To maximize space, the hybrids sit at different radial positions depending on hybrid Z position. As we move along Z, we lose 1 analog cable and gain 1 digital cable for each hybrid. We kept the castellated shell shape constant with Z, but put spacers underneath those hybrids at smaller Z to provide additional space for the larger stacks of analog cables.

4.3.3 Finite element analysis of the Layer 0 mechanical structure

4.3.3.1 Mechanical FEA

The high precision required in the Layer 0 silicon support structure implies that this very light structure must also be very stiff. The design process must be accompanied by detailed structural analysis using FEA methods.

The design of the Layer 0 support structure was modeled using the ANSYS 7.1 FEA software. The model geometry was generated using Unigraphics NX CAD system and then transferred into ANSYS via Parasolid files. The model includes detailed representations of all of the major structural parts and covers the complete length of the Layer 0 silicon support structure. This structure is symmetrical about Z = 0 and only one half is described and shown below.

There are four major parts to the structure. In the silicon sensor region this includes the inner carbon fiber tube, the outer carbon fiber six-sided castellation, the layers of epoxy adhesive used in the structure, the layers of kapton and epoxy between the structure and the sensors and the actual silicon sensors. The orthotropic properties of all of the fiber structures were determined from tensile testing and composite lay-up theory. Care was taken to ensure that the orthotropic properties were correctly assigned at each element. To keep the model to a manageable size, the stacks of kapton and epoxy layers were not modeled in detail. These parts were represented by elements with 'dummy' material properties such that they have equivalent weight and bending stiffness to the actual structures.

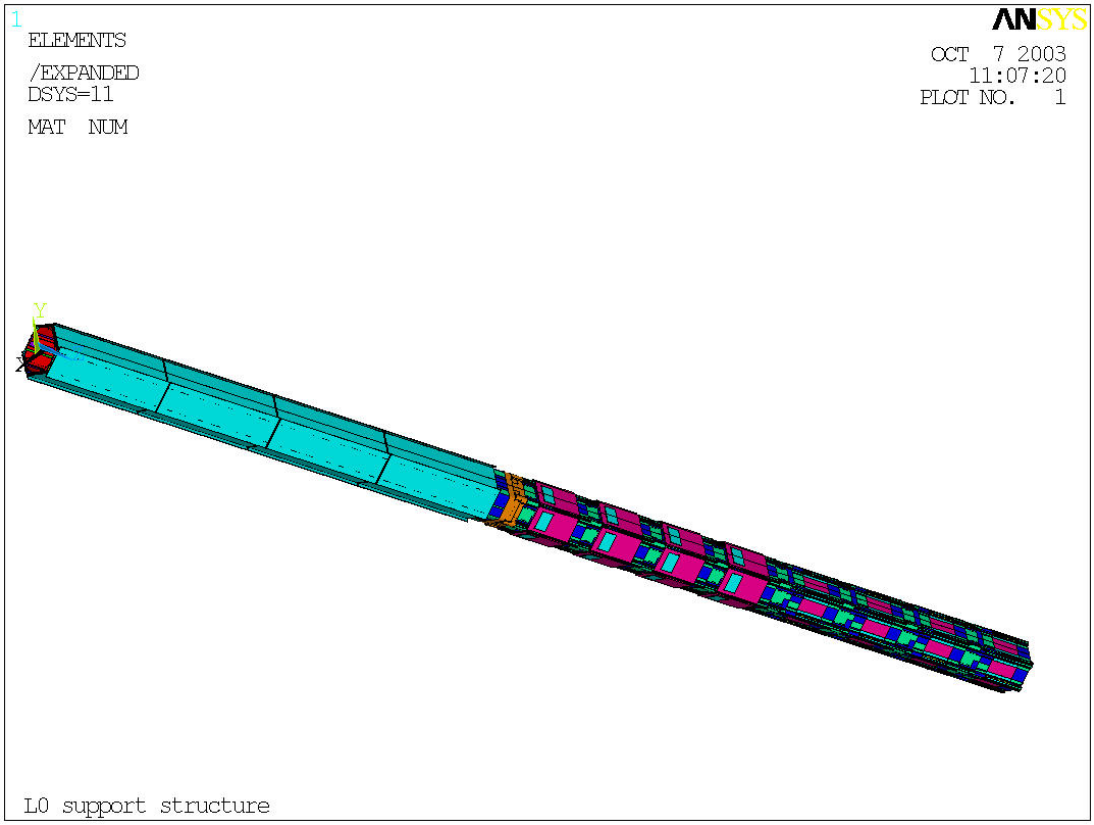

Figure 21 - FEA model of the Layer 0 support structure.

The model was loaded by gravity only. Other loads, such as the weight of the analog cables and the coolant will be added later. Given the symmetry of the structure and the loads, only one half of one end of the structure was actually modeled. ANSYS has a display option that allows one to expand the whole structure and this is used in all figures below. The overall model is shown in Figure 21. Details of the sensor end are shown in Figure 22, Figure 23, and Figure 24.

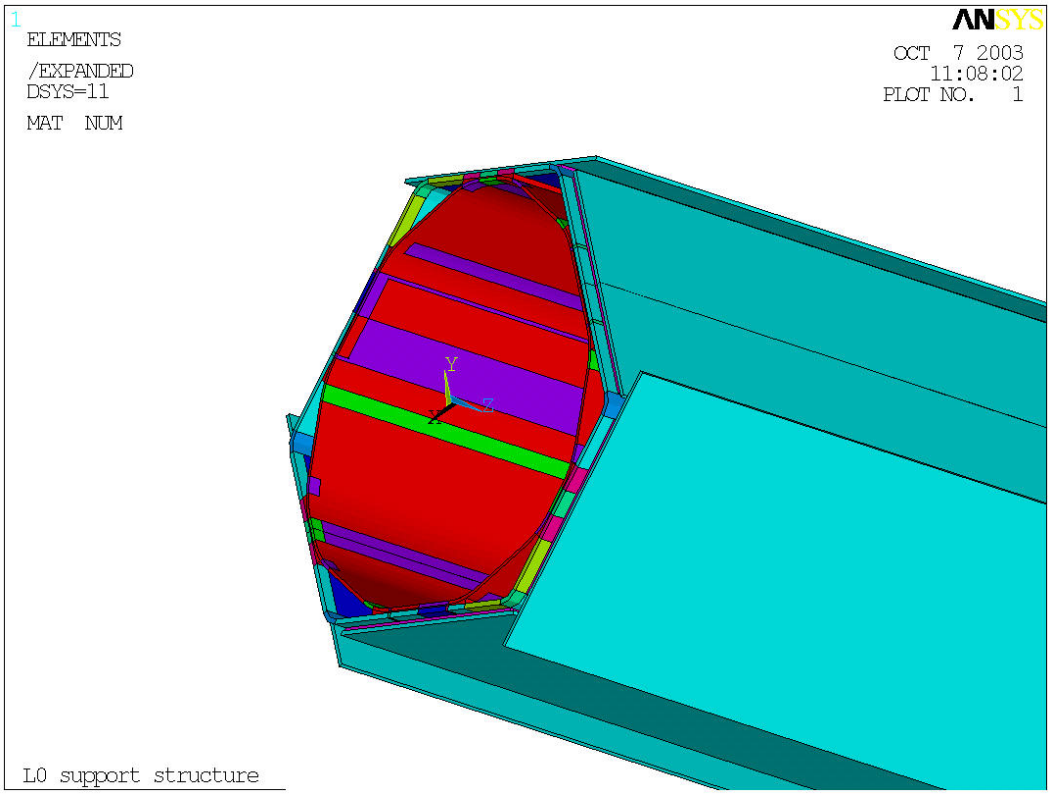

Figure 22 - Element structure at Z = 0 in the sensor region.

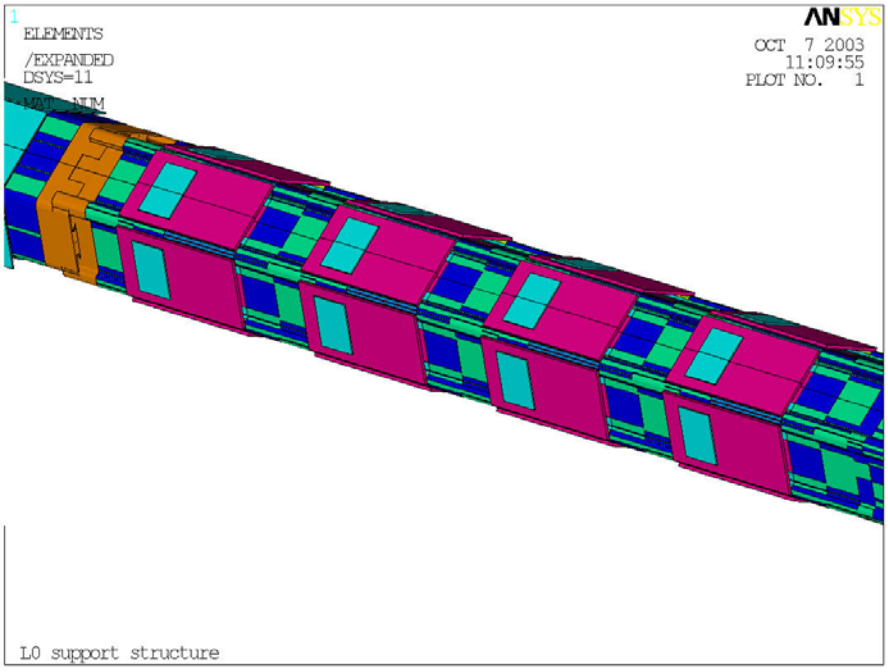

Figure 23 - Element structure at the hybrid region.

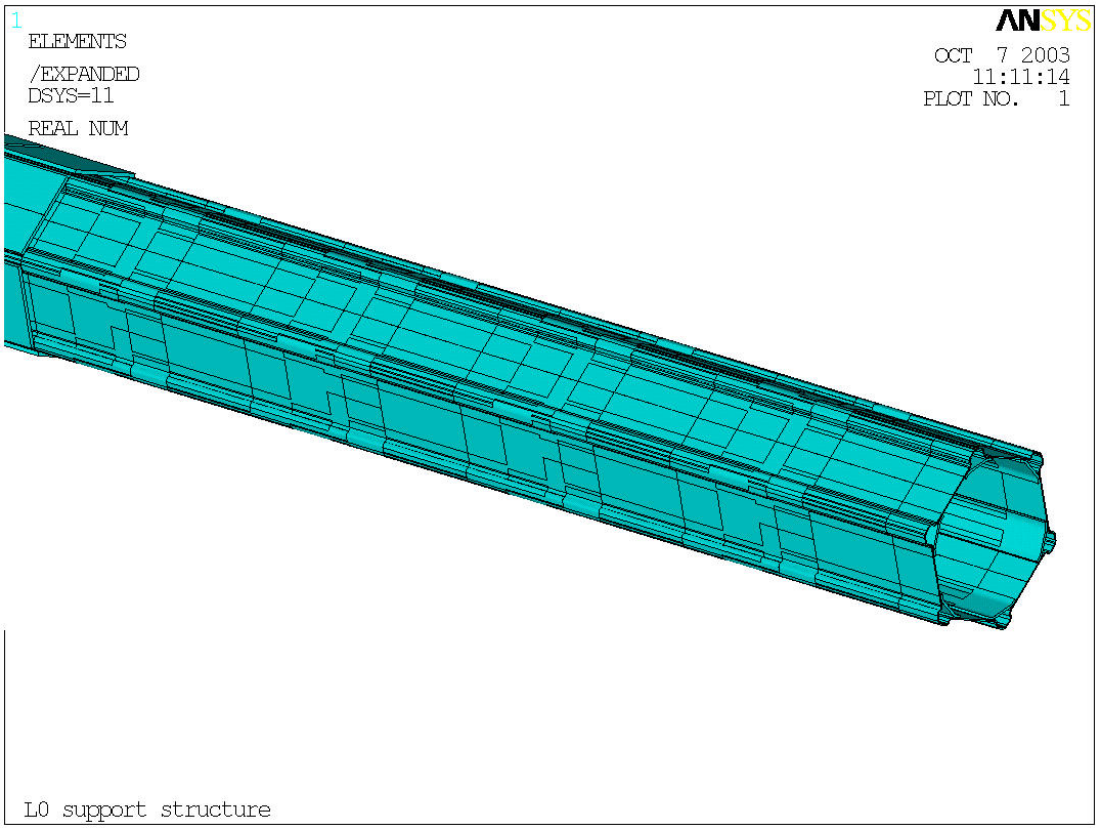

Figure 24 - Elements structure at the support extension to Z = 803 mm.

The deflection of the structure due to its own weight is shown in Figure 25 and Figure 26. The maximum sagitta of the structure is 31.1 μm. This is with simple support conditions at Z = 830 mm.

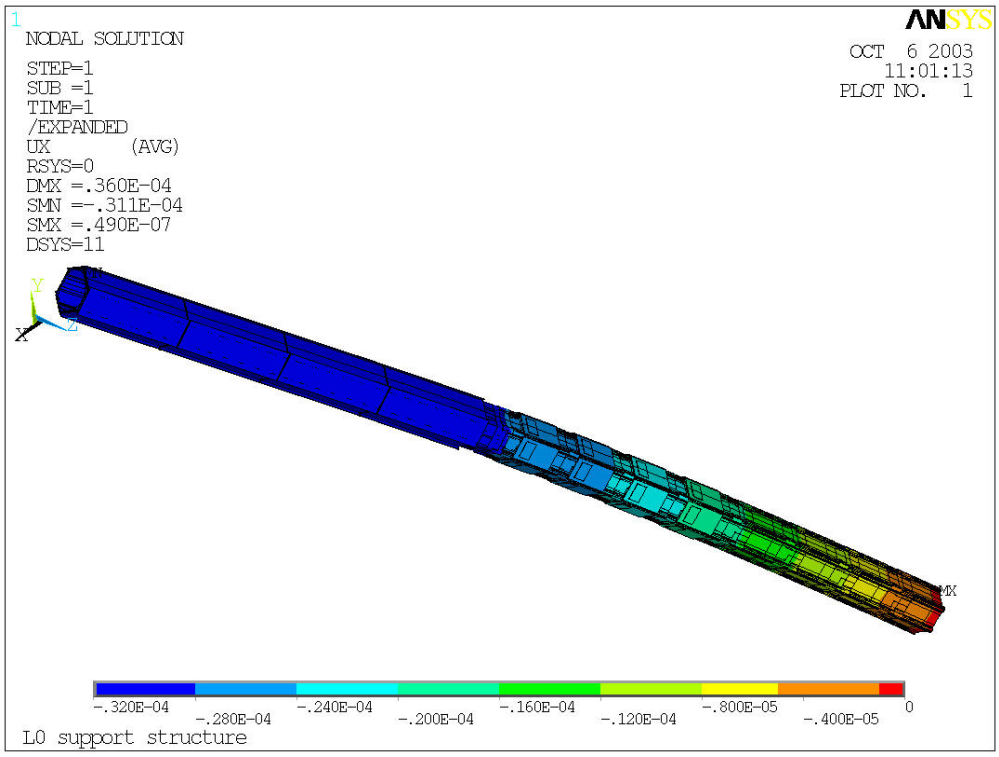

Figure 25 - Deflection of the Layer 0 structure under its own weight.

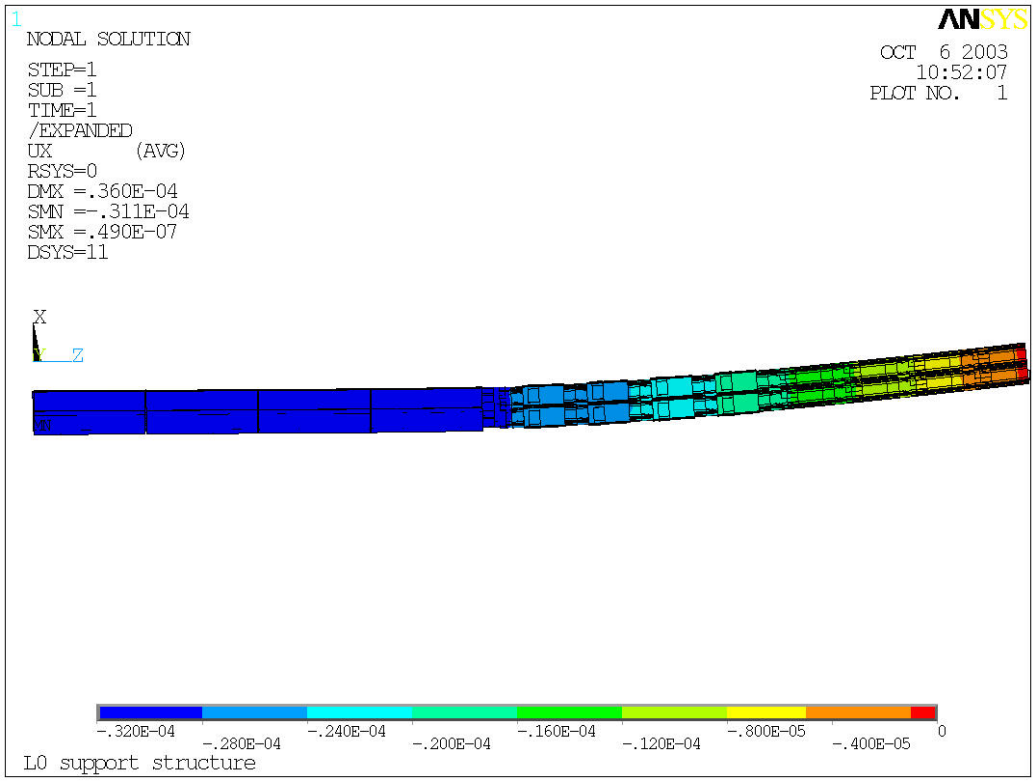

Figure 26 - Deflection of the Layer 0 structure under its own weight.

The weight of the cooling tubes and coolant will add about 14% to this giving a sagitta of 35.5 μm. The cables will add another few percent.

Changing the support conditions can dramatically change the above sagitta. E.g. adding at support at Z = 0 mm would reduce the sagitta to 0.92 μm. Moving the two end supports inwards would also make a major reduction. Any proposed support condition can be quickly checked using this FEA model. The proposed design may include an outer protective cylindrical shell made from carbon fiber composite. This will contribute to the bending stiffness although it would require connections to the inner structure using several membranes to make a major difference. Again, such a structure can be added easily to the FEA model.

4.3.3.2 Thermal FEA

No thermal FEA has been done as yet. Based on experience with this on the Run IIb L0 and L1 structures it is clear that there should be no major cooling problem with this new Layer 0 structure. As the sensors will produce very little heat, they will operate at very close to the temperature of the coolant flowing through the sensor region. This is determined only by heat generated by the hybrid region(s) through which this coolant passes prior to reaching the sensor

region and by the coolant properties and flow rate. With the coolant entering the system at –9 C, there should be no problem in keeping the sensor temperatures below 0 C.

4.3.4 Support structure fabrication

The sensor and hybrid support structure shells are fabricated by wrapping carbon-fiber/epoxy pre-preg material around mandrels that are machined to the specified cross-sectional dimensions. The outer shells are 6 ply lay-ups, with fiber orientations of $[0°/+20°/–20°]_s$. The inner shells are 4 ply lay-ups, with fiber orientations of $[0°/90°]_s$. The cross-sections of the proposed Layer 0 shell assemblies are shown in Figure 27 and Figure 28. The change in geometry that occurs between the sensor and hybrid regions requires that a manifold be used to join the shell assemblies and cooling tubes, similar to the approach taken for the L1 support structure for Run IIb.

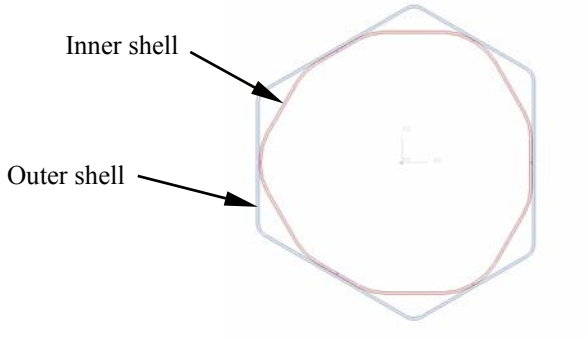

Figure 27 - Layer 0 sensor support shells.

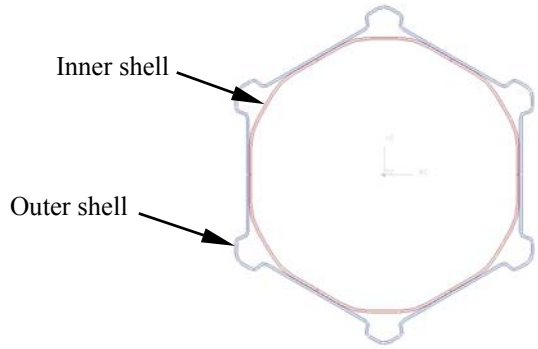

Figure 28 - Layer 0 hybrid support shells.

Standard vacuum/autoclave procedures are employed in the lay-up of the carbon fiber shells, as recommended by the material manufacturer, and further refined during the fabrications of the Run IIb L0 and L1 prototypes. The detailed steps to lay up the carbon fiber structure and to

quality control the finished parts are described in the Technical Design Report for Run IIb[25]. Figure 29 shows the first layer of carbon fiber wrapped on the Run IIb castellated mandrel and Figure 30 shows the completed/cured prototype castellated shell. The proposed Layer 0 structure lends itself to the production techniques developed for the Run IIb L0 and L1 support structures.

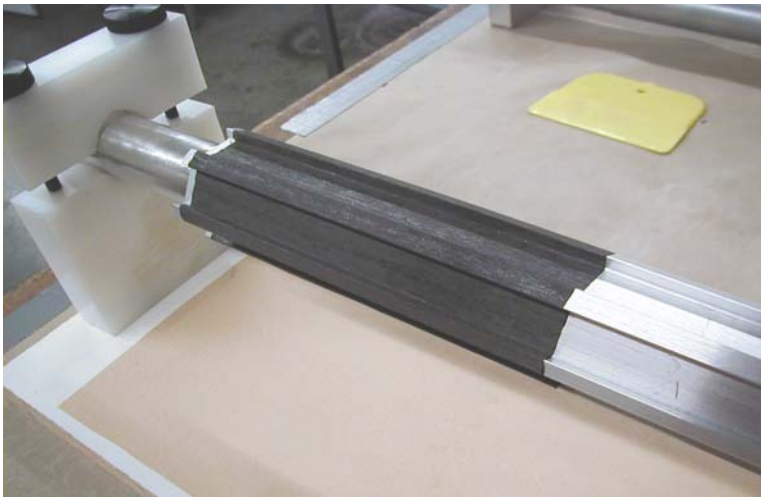

Figure 29 - Carbon fiber wrapped on castellated mandrel.

Figure 30 - Finished prototype Run IIb castellated shell.

[25] DØ Run IIb Upgrade Technical Design Report, FERMILAB-PUB-02-327-E, December 2002.

4.3.5 Support structure shell assembly

The sensor placement surface must be controlled to very high precision. In order to precisely fix the sensor placement surfaces at the specified positions, the outer shell is adhesively bonded to the inner shell using precision tooling. The sensor cooling tubes run between, and are adhesively bonded to, the outer and inner shells. A cross-section of the assembled Layer 0 sensor inner/outer shells, including the sensor cooling tubes, is shown in Figure 31.

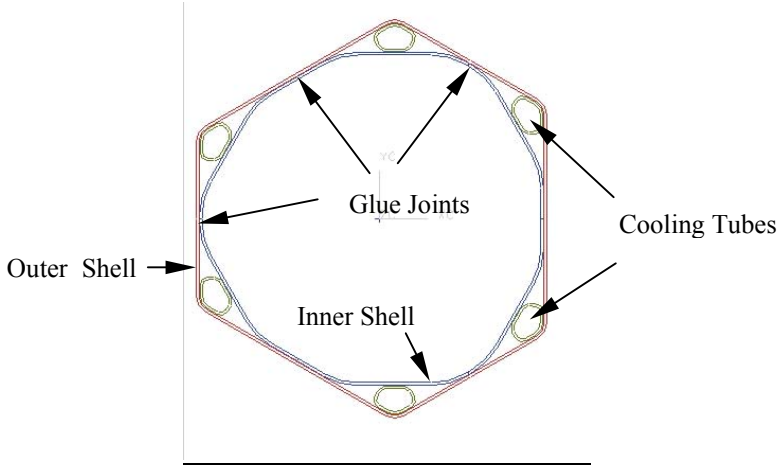

Figure 31 - Layer 0 sensor support structure shell assembly.

The shells will be joined using a B-staged epoxy film adhesive. The cured film thickness is currently specified as 25 μm (.001”). Assembly procedures developed for the Run IIb support structures can be readily adapted to accommodate the new geometry of the sensor and hybrid support shells. The detailed steps to assemble the carbon fiber structure, which were verified with the assembly of the Run IIb prototypes, are summarized below. Figure 32 shows the assembled Run IIb L0 prototype that includes a co-bonded kapton/copper-mesh ground plane.

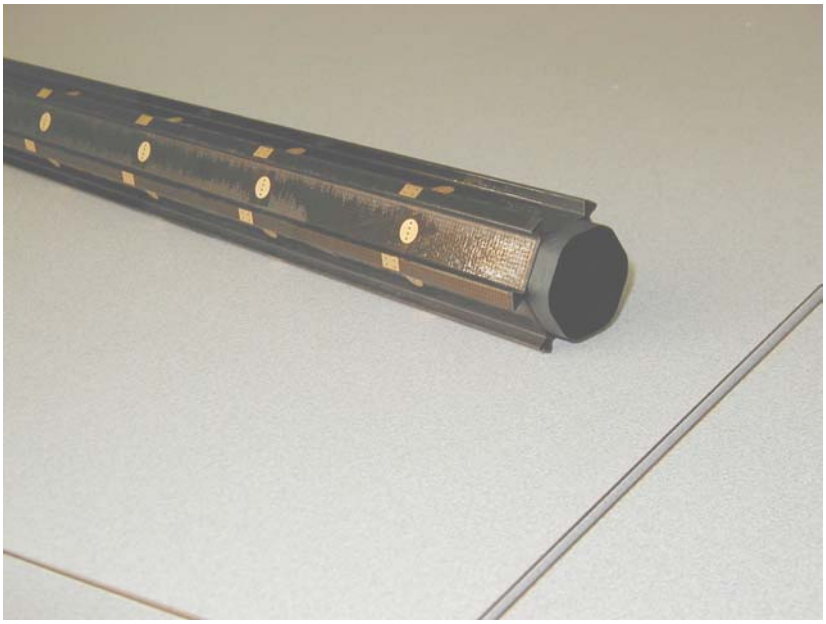

Figure 32 - Prototype of the Run IIb L0 inner and outer shell assembly.

The inner shell is slid onto a precision mandrel. Strips of film adhesive are then applied to the mating surfaces of the inner shell (the material has a light tack at room temperature). Strips of film adhesive are applied to the inner surfaces of the outer shell where the cooling tubes are bonded. The outer shell and cooling tubes are then slid over the inner shell. Once the parts have been properly positioned a set of precision steel pressure-bars is installed onto the mandrel. The bars have a step machined in the bottom that defines the overall distance between the mandrel surface and the sensor placement surfaces on the outer shell.

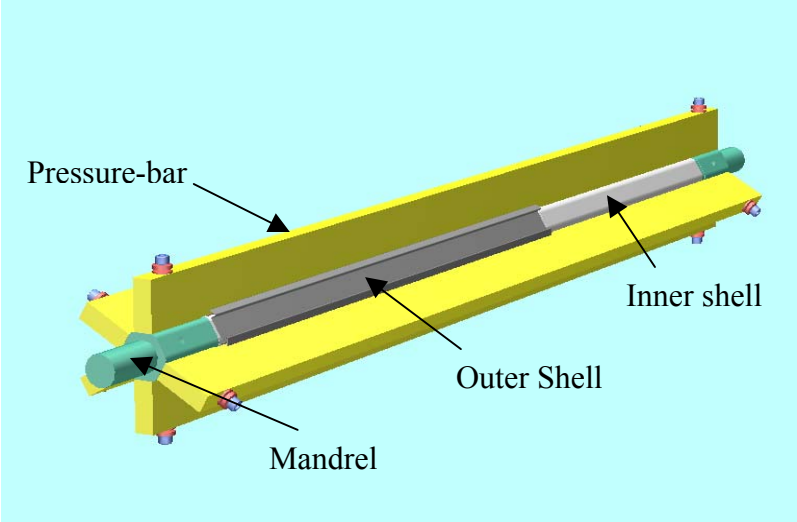

Figure 33 - Run IIb L0 shell assembly fixture.

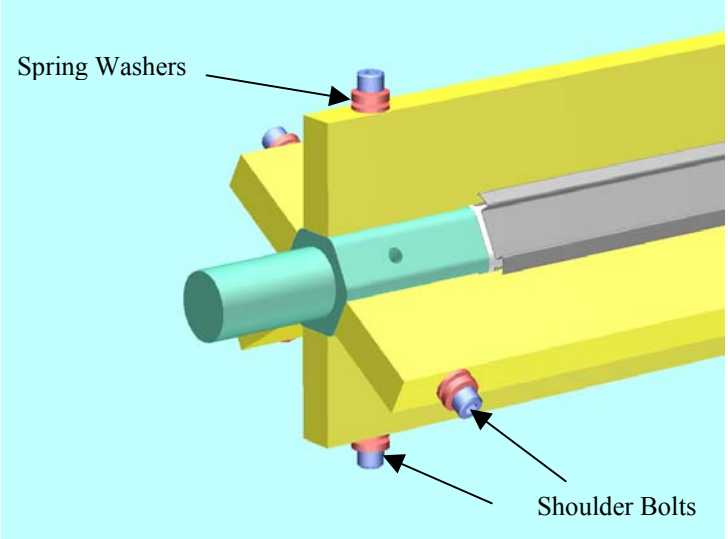

Figure 34 - Detail of Run IIb L0 shell assembly fixture.

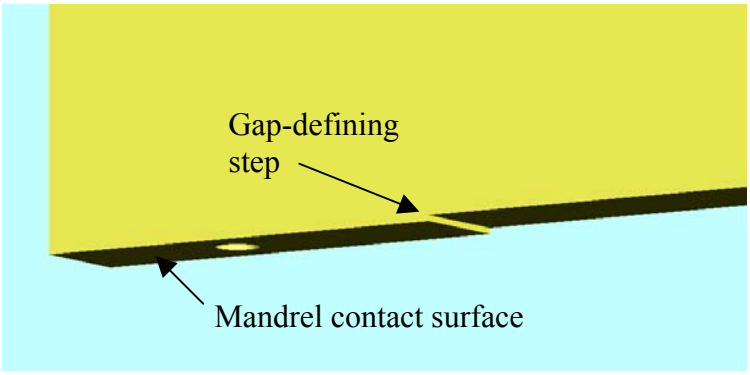

Figure 35 - Pressure Bar.

Shoulder bolts combined with spring washers are used to lightly clamp the bars to the mandrel (Figure 34). The entire assembly is placed into the oven in an upright position to avoid gravitational sag of the tooling. As the temperature ramps up, the film adhesive begins to soften and flow under the pressure of the tooling. At several intervals, the shoulder bolts are tightened to increase the pressure, until finally the bars are solidly stopped against the precision surfaces of the mandrel. The pressure-bar step dimension is chosen such that the adhesive film thickness is reduced by a pre-determined amount during the cure. Preliminary tests bonding kapton film suggested an appropriate thickness reduction to be ~50% in order to insure a consistent, void free bond line. This was verified during the assembly of several prototype pieces for Run IIb.

4.3.6 Sensor – hybrid modules

4.3.6.1 Design

The Layer 0 module consists of a sensor coupled to analog cables and a hybrid. The basic layout of a Layer 0 module is shown in Figure. Four module types will be required. The two modules closest to Z = 0 will use 70 to 75 mm long sensors while the two further from Z = 0 will use 115 to 120 mm long sensors, with a total length of 380 mm. The same hybrid design will be used for all modules. Minimal changes will be required to adapt the hybrid developed for Run IIb to this application. Analog cables will be required in four lengths, from 340 mm to read out the sensor closest to Z = 0 down to 145 mm to readout the sensor furthest from Z = 0. The analog cables developed for Run IIb are a suitable design for this application. Lengths will need to be altered (reduced from the Run IIb design) and a fan-out to the wider sensor strip pitch will need to be incorporated at the sensor end of the cables. The main run of the cables and the hybrid end can remain unchanged.

There are no physics drivers in the alignment of the components within the modules themselves – this is driven entirely by the tight space constraints. Radial space is at a premium so it is critical that all joints contributing to stack-up of components in these critical areas is well understood and controlled. Two of the most critical regions are the areas of the wire bonds from the analog cables to the sensors and from the cables to the hybrids. Four glue joints are required to build the stack: sensor/hybrid – glue - bottom spacer – glue - bottom cable – glue - top spacer

– glue - top cable. For the joints between the cable spacers and the cables it is critical that we have no voids under the bond pads. For all joints it is critical that we maintain as thin a glue line as possible and prevent run-out of adhesive over the bond pads. Significant progress was made during the R&D phase of the Run IIb project in fixturing and procedures to accomplish this. Since the cable, sensor and hybrid designs are essentially identical, that experience is directly applicable and we foresee minimal changes required in both tooling and procedures. The module assembly process is outlined in the Production section of this document. The basic strategy is to use fixtures with alignment dowels to locate the sensor and cable to one another and the hybrid and cable to one another, with vacuum hold-down of the sensor and hybrid during bonding. Similar tooling is used to assemble the cable pairs prior to attaching them to the sensor and hybrid. Transverse tolerances of 50 to 75μm are expected, which is adequate.

4.3.6.2 Module installation and alignment

The installation and alignment of modules present challenges quite similar to those met by CDF in assembly of their L00 detector. The structure extend 830 mm from Z = 0 on each side and we anticipate that modules will likely have to be installed on a complete 1.6 m long structure. At the same time the diameter is only 32 mm, making for a 50:1 aspect ratio. During module installation significant forces, relative to module and structure weights, will need to be applied to create large area thin glue joints under the sensors and in the thermal path between the hybrids and coolant. These loads will need to be reacted both by the structure itself and by additional supports, such as stiff interior mandrels and support at Z = 0. Deflection of the structure during gluing operations needs to be understood in the context of alignment errors introduced by "freezing" deformations into the assembly as modules are mounted. Preliminary studies of the Run IIb L0 structure indicated that these effects are at levels that could potentially affect final detector performance.

While a detailed plan is yet to be developed, the basic outline for module installation is as follows. The carbon fiber support structure will be held at two or three points, depending on whether the modules are installed on a full-length structure or separately on two half-length structures. Support points will be kept as close together as possible, namely at Z = 0 and just outboard of the last hybrid near Z = 560 to 580 mm. This will minimize the deflections of the structure during the loading required for module installation. Sensors will be held from their top surface with flat vacuum chucks to remove, to the extent possible, the inherent bow of the sensors. These vacuum chucks will be positioned using commercial XYZ stages with a CMM used for optical feedback to the operator. In this way sensor fiducials can be used to align the sensor to the ideal locations to within a few μm. The tooling requires one rotational degree of freedom, which can be implemented either using a commercial rotary stage or independent transverse positioners at the two ends of the vacuum chuck. The other two rotational degrees of freedom are "dead reckoned" by the tooling, *i.e.* the sensor plane is made parallel to the ideal plane by construction of the tooling. The latter may prove to be unacceptable if the deflections of the structure during module installation are too large. In this instance double leaf springs can be implemented at each end of the vacuum chuck. These provide precisely vertical motion

without rotation so that each end of the sensor can independently come to the appropriate elevation. An independent support holds the hybrid until the sensor glue joint cures. At this point the hybrid is moved to its final location with the analog cables carefully dressed into place and the hybrid is glued in place. Module installation can easily proceed at a rate of 2 per day (one at each end) allowing for complete installation in 5 weeks.

The alignment constraints are driven primarily by inclusion of this layer of silicon in the Silicon Track Trigger (STT). The STT does not have any Z information available to it; therefore any angular misalignment of the strips to the beam axis degrades the resolution. Since the STT uses the beam spot, rather than a reconstructed primary vertex, the impact parameter resolution for the trigger is limited by the size of the beam spot, about 30 μm. Based on trigger efficiency analyses it is estimated that the trigger performance will not be significantly degraded if the strips are aligned to the beam axis to 600 μrad or better. We anticipate, based on prior experience, that the sensors within a ϕ sector can be aligned to each other within 5μ in the plane of the sensors and 30 to 50 μm out of the plane. From sector to sector it should be possible to establish coordinate systems to 50 μm over the half-length of the structure (830 mm) and similarly between the two ends of the structure. In total this amounts to less than ¼ of the allowable tolerance. The remainder allows for alignment of the detector package to the existing Run IIa detector and the Tevatron beam axis.

4.3.7 Materials and radiation lengths

Results of a preliminary calculation are given in Table 9. Details will be updated as designs are developed. To ensure adequate space will be available as the design evolves, conservatively high sizes have been assumed for individual components and elements.

Table 9 - Layer 0 materials and number of radiation lengths.

Average radiation length in L0 tracking volume for particles in the normal direction

Objects	Material	Radiation length	Average radius	Length	Width	Phi coverage (degrees)	Thickness	Weighted thickenss	Average % of X0
Sensors	Silicon	94	17	380	20.216	360.00	0.32	0.3611	0.384
Analog cable									
Kapton substrate	Kapton	284	19	380	13.948	241.88	0.0750	0.0539	0.038
Copper (0.01x0.005 mm^2)	Copper	14.3	19	380	13.948	241.88	0.0015	0.0011	0.015
Gold (0.001x0.001 mm^2)	Gold	3	19	380	13.948	241.88	0.0003	0.0002	0.014
Kapton/copper mesh									
Kapton substrate	Kapton	284	19	380	13.948	241.88	0.0300	0.0216	0.015
0.005 mm copper (25%)	Copper	14.3	17	380	106.81	360.00	0.0050	0.0050	0.035
0.001 mm gold (25%)	Gold	3	17	380	106.81	360.00	0.0010	0.0010	0.033
Support structure	CF/epoxy	250	17	380	106.81	360.00	0.6400	0.6400	0.256
Coolant + Cooling tube		350	16.5	380	42	145.84	1.0000	0.4051	0.116
								Total	**0.907**

Average radiation length in L0 hybrid region for particles in the normal direction

Objects	Material	Radiation length	Average radius	Length	Width	Phi coverage (degrees)	Thickness	Weighted thickenss	Average % of X0
Hybrids (assuming average radiation length 2.5%)	Varies	40	18	35	18.9	332.40	1.00	1.0000	2.500
Digital Cable (assuming 2 calbes over full length)									
Kapton base	Kapton	284	19	35	14.8	255.36	0.50	0.5000	0.176
Copper traces	Copper	14.3	19	35	11	193.74	0.12	0.0646	0.839
***Analog Cable**									0.068
***Kapton/copper mesh**									0.068
***Support structure**									0.256
***Coolant + Cooling tube**									0.116
* Same as sensor region								**Total**	**4.023**

4.4 Installation and Alignment at DØ

We assume a fully completed and checked Layer 0, including beam tube, will be shipped to DØ from the Silicon Detector Facility (SiDet). That means that Layer 0 has been fully checked electrically, that cooling passages have been checked and are known to be leak-free, that fiducials are available and a sufficient number of them are accessible, that silicon positions have been measured with respect to fiducials, and that the beam tube is clean and leak-free. A suitable protective enclosure with dry gas purge and acceleration-limiting support would be provided.

The beam tube and ends of silicon support structures should provide adequate reference points for transverse and longitudinal positioning at DØ. The end membranes of the silicon support cylinders of the present silicon tracker carry V-STAR fiducials whose locations, in principle, are known in the silicon and fiber tracker coordinate systems. Locations of centers of the 1.875" holes through support cylinder end membranes are also known.

Means of orienting Layer 0 in azimuth remain to be developed. In practice, that appears to mean we either need features which allow azimuthal orientation to be based upon gravity or we need to rely upon V-STAR targets carried by the Layer 0 support structure.

Depending upon the final installation method chosen, digital cables may need to be enclosed by and supported by temporary extensions to the new beryllium beam tube. One plausible installation method is described.

4.4.1 Preparations

At DØ, four shielding blocks need to be removed from the roof of the collision hall to provide a path for lowering Layer 0 into the collision hall. Silicon needs to be warmed to room temperature. Cooling passages need to be drained and appropriate coolant flow areas dried. Isolation valves for accelerator vacuum need to be closed outside each end calorimeter. End calorimeters need to be opened and access scaffolding needs to be installed.

Removal of existing equipment relies upon methods and fixturing used during original silicon and beam tube installation.

The Run IIa beryllium beam tube is disconnected at its two flanges. Then the bellows assembly and flange of at least one of the stainless steel beam tubes through an end calorimeter is cut off. Supports from the outermost H-disk enclosures to the beryllium beam tube are removed. Existing fixturing, which attaches to the solenoid at 12 o'clock, provides support to the beryllium beam tube as the tube is slid into the beam tube of an end calorimeter. End membranes of the silicon support cylinders support the beryllium tube until it engages the fixturing. The beryllium tube is moved fully into the beam tube of the calorimeter and stored there temporarily.

The outer H-disks are un-cabled, un-plumbed, and then removed using fixturing which attaches to the solenoid. Whether the inner H-disks need to be similarly removed isn't clear yet.

4.4.2 Removal of existing beam tube

At this point, we close the end calorimeter with beryllium beam tube to allow extraction of the beryllium tube from the outer calorimeter end. That is the inverse of installation, but installation was in the DØ assembly hall, rather than collision hall. Shielding outside the calorimeter needs to be opened to provide an access path. Portions of the Tevatron beam tube as far as the vacuum isolation valve near the low-beta quads will likely need to be removed. We have been advised that creates sufficient space to allow the 96.6" long beryllium tube to be removed intact, but need to confirm that. The beryllium portion is nominally 93.6" long. If necessary, methods to cut the beam tube (used on the DØ Run I beryllium tube) without generating filings or chips are known. Our preferred solution is to remove the beryllium tube intact.

4.4.3 Layer 0 mechanical installation

Layer 0 is brought from SiDet to DØ and lowered into the collision hall. The detailed path within the collision hall to the outer end of a calorimeter still needs to be investigated. If necessary, we will investigate an alternative path via the Tevatron tunnel.

The nominal length of the Run IIb beryllium beam tube is 72". Twenty-four digital cables extend a short distance (possibly 0 and probably not more than 12") past each end of the beam tube, but are flexible. The plan is to move the Layer 0 assembly into the end calorimeter beam tube from the outer end. The outside diameter of the silicon support structure is approximately 1.795". The inside diameter of the end calorimeter beam tube is nominally 1.944", which leaves a radial clearance of 0.074". The Layer 0 assembly will carry a protective outer layer. If necessary, the stainless steel beam tube through the end calorimeter can be removed to provide greater radial clearance.

To aid in installation, we plan to use fixturing similar to that used previously for installing the Run IIa beam tube. The fixturing will need to extend closer to the end of fiber tracker barrel 1. Its adjustments of position and angle are likely to depend upon micrometers, rather than the methods of Run IIa (manual placement with locking screws).

Our proposal is to support the Layer 0 structure from the new beryllium beam tube during installation. Figure 36 shows the calculated deflection of the 200 gram beryllium beam tube with 150 grams of Layer 0 weight transferred to the tube at Z = –31.496" and 150 grams at +31.496". The beam tube is supported, as it would be within existing silicon, at Z = ±32.64". Straightness of the Layer 0 structure, with simple support at its two ends, is not altered by deflection of the beam tube provided contact is avoided other than at support locations. Maximum bending stress in the beryllium tube is low, about 137 PSI.

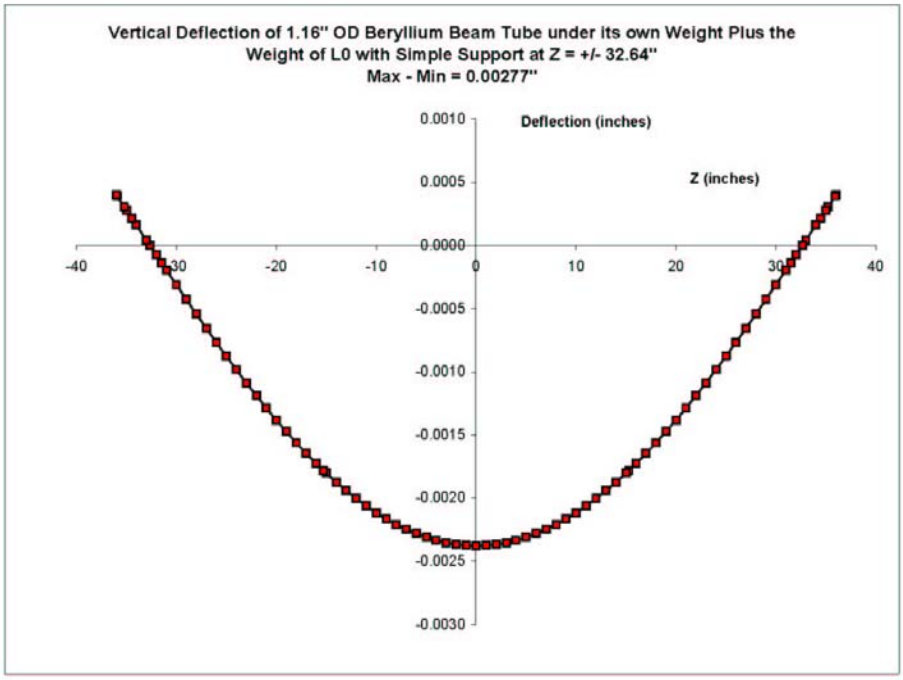

Figure 36 - Deflection of the beryllium beam tube under its own weight plus that of Layer 0. Sagitta relative to ends = 0.0028".

During installation, we plan to cantilever the beam tube plus Layer 0 load from one end of the beam tube. Deflection of the beam tube while held near one end, between Z = 34" and Z = 35", is shown in Figure 37. Deflection at one beam tube flange is 0.1031". Stresses in the beryllium are acceptable. Maximum amplitudes of bending, shear, and principal stresses (not all at the same Z) are 1814 PSI, 492 PSI, and 1814 PSI, respectively.

While that deflection, at first glance, may seem large, it is the deviation from a straight line that matters. Figure 38 shows deflection results with the cantilever angle and offset set so that Layer 0 support elevations are at Y = 0. Then the maximum beam tube deflection relative to the nominal Layer 0 axis is 0.0154". Provided the beam tube is oriented with its natural bow (Figure 12 and Figure 13) downward, no contact should occur between the beam tube and Layer 0 during Layer 0 installation other than at Layer 0 support locations. We would provide additional support to the beam tube and Layer 0 from the end furthest from the cantilever fixture at the earliest opportunity. In all likelihood, that would rely on an identical fixture.

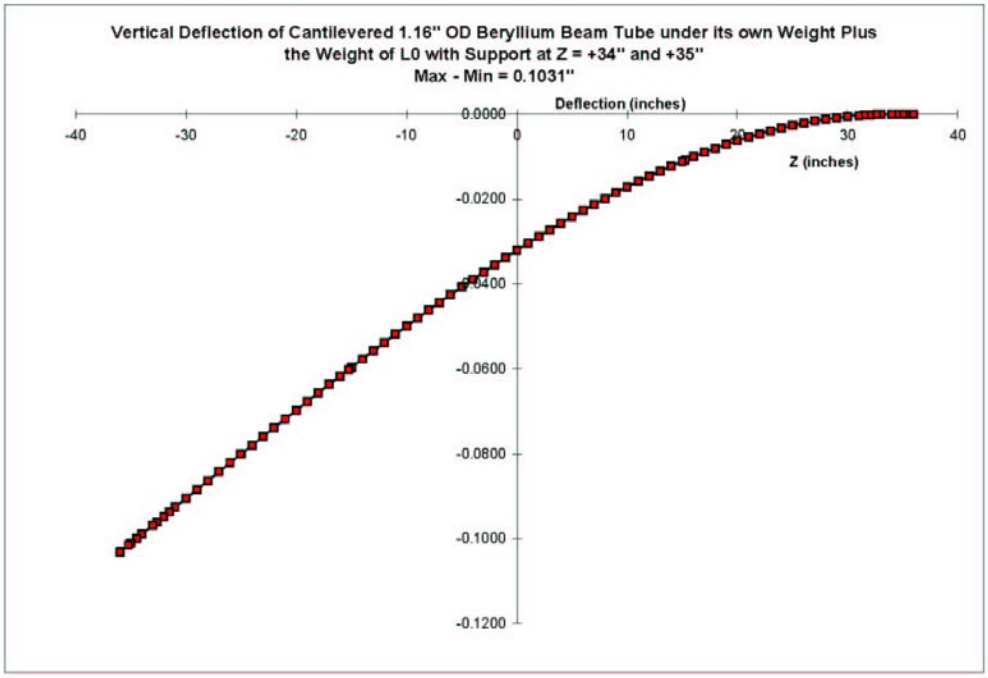

Figure 37: Deflection of the beam tube under its own weight plus that of Layer 0 with cantilevered support

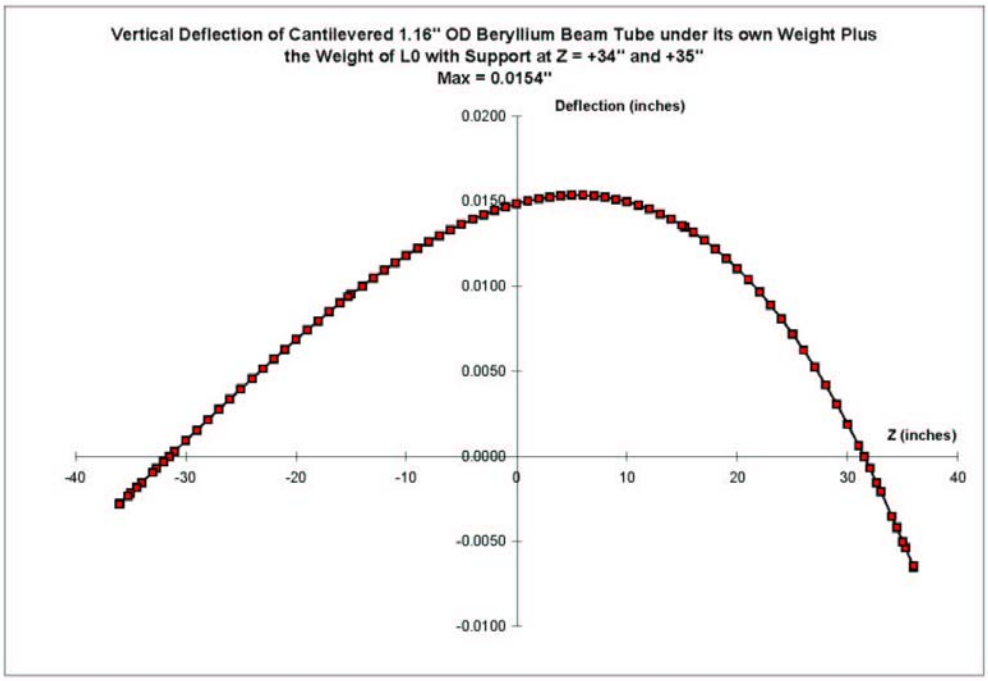

Figure 38 - Deflection of the beam tube under its own weight plus that of Layer 0 with cantilevered support and adjustment of cantilever angle and offset.

A more detailed analysis of installation issues remains to be made. For example, the weight of beam tube extensions to enclose and support cables and the weight of the cables themselves have not been included. Corrections for these should be small. We also need to understand the details of local forces on the beam tube at the cantilever location and the design of cantilever apparatus with sufficient Z motion. In addition, the Layer 0 beam tube will still extend 13" within the end calorimeter beam tube when the Layer 0 beam tube begins to enter the support cylinder of existing silicon. When the Layer 0 beam tube clears the calorimeter, it extends just through the opening in the outermost F-disk. That implies an intermediate support stand (or equivalent) will be required until the cantilever mechanism can be engaged. Intermediate support stands were used during installation of the Run IIa silicon.

Once Layer 0 and the beam tube are in place, support is provided from the Z = 830 mm membranes of the existing silicon support cylinder. We haven't determined yet whether Layer 0 and the beam tube will be supported individually or whether the beam tube will support Layer 0. In any case, Layer 0 transverse, longitudinal, and azimuthal orientations need to be set by the support connections.

4.4.4 Beam tube leak checking

The new beryllium beam tube was baked out and helium leak checked at Brush-Wellman Electrofusion. An additional helium leak check was performed by Particle Physics Division technicians after receipt of the beam tube at Fermilab; no leaks were detected. The beam tube is in storage at DØ under a dry nitrogen purge. A final bake-out, helium leak check, and Beams Division acceptance certification are needed prior to beam tube installation within silicon structures at SiDet. A final leak test will be performed at SiDet after the beam tube is in place within the silicon structures. Except for short interruptions during installation processes at SiDet and DØ, a dry nitrogen purge will be maintained through the beam tube until it is connected to accelerator vacuum. A dry air purge will be established and maintained outside the beam tube and through the silicon region as soon as practical.

Details of beam tube leak checking at DØ, in coordination with the Beams Division, remain to be developed. For Run IIa installation, beam tube leak checking required opening and closing End Calorimeters and other DØ structures multiple times. While similar procedures are likely to be needed for Layer 0 installation, we will try to minimize the number of times large structures are moved.

4.5 Mechanical Infrastructure at DØ

Cooling and dry gas systems after installation of Layer 0 will be essentially unchanged from those currently in use. Cooling and dry gas connections now provided to the H-disks (which will no longer be in use) will be transferred to Layer 0. While some number of additional Cryo control system input modules are likely to be required, for temperature measurements in particular, the basic control, monitoring, and interlock systems will also remain unchanged.

4.5.1 Cooling system

Silicon is cooled by a circulating, de-ionized, mixture of ethylene glycol and water. Normal coolant temperature is -9^{o} C. To help ensure the coolant will not freeze, the ethylene glycol concentration was chosen to provide a coolant freezing point of -15.3^{o} C. Coolant total flow rate is about 11 GPM. Coolant temperature rise through the silicon region is about 1^{o} C.

The DØ silicon cooling system was designed to operate reliably with minimal attention and reliance upon controls. Refrigeration is provided by a set of two chillers, each with a pump for circulating coolant. Each chiller has a specified refrigeration capacity of 4600 watts at -10^{o} C (a capacity of 5500 watts for each of the chillers was measured at Fermilab). One chiller is operated at any given time, with the second connected and ready for operation. Each chiller has an internal temperature controller; the controller of the chiller in use sets the system coolant temperature. Flow to and from silicon is set by manual valves with the aid of rotameters and electronic flow meters; once set at operating temperature, the valves have not required readjustment. Sub-atmospheric pressure in the silicon region is obtained by drawing coolant through the silicon coolant passages from a storage tank maintained at atmospheric pressure.

The system design and reliability have been demonstrated through more than 20000 hours of successful operation.

The same basic system would be used after installation of Layer 0. Existing nozzles on coolant supply and return manifolds, now used for H-disk connections, would be used for Layer 0 connections. In the present silicon tracker, supply and return connections for each silicon device are at the same end of the silicon. Layer 0 differs in that each cooling passage would receive supply from one end of the silicon and would return flow to the opposite end. We have examined the consequences of this flow configuration and concluded that there is negligible impact on flows rates.

4.5.2 Dry gas system

Minimum temperature within the silicon region is nominally -10^{o} C, which is roughly 30^{o} C colder than the normal temperature of the DØ collision hall. Typical dew point within the collision hall is $+10^{o}$ C. To prevent water condensation, dry air flow of 25 SCFM is provided to each end of the silicon region. Of the 25 SCFM, 1 SCFM flows into each H-disk enclosure, 1 SCFM into the silicon barrel region, and the remainder between the silicon support cylinder and the fiber tracker. Measured dew points within all silicon regions are typically below -55^{o} C.

The existing dry gas purge and process control systems will be used after the addition of Layer 0. Purge gas supply for the innermost H-disk enclosures, which will no longer exist, will be re-directed to Layer 0.

Dual, redundant air compressors with dual air driers supply dry air. Gas cylinders and tube trailers provide a back-up supply of dry gas should a failure occur in the compressor system. Automatic switchover to back-up sources is based upon supply pressures, supply gas dew points, dew points measured at ten locations within the silicon region, and the presence of AC power. Various additional software-based conditions can initiate an “emergency warm-up” and switchover to back up dry gas supplies.

The dry gas source was shown by a ‘What-If’ failure analysis to be “failsafe”. The dry gas system remains operational during all probable failure modes or has enough of a dry gas reservoir to continue to purge the detector until it is warmed above building dew point temperature. The purge source is reliable through extreme summer (40^{o} C, 100% relative humidity) and winter (-35^{o} C) weather. The system is capable of delivering 60 SCFM of dry air purge. The maximum dew point temperature of the delivered gas is -60^{o} C. The compressors, dryers, and cooling system will require appropriate maintenance after five years of continued service, but that would be necessary in any case. The system design and reliability have been demonstrated through more than 20000 hours of successful operation.

4.5.3 Monitoring, interlocks, and controls

Primary interlocks are based upon hard-wired devices (pressure switches, flow switches, temperature switches, dew point meters) that are wired for fail-safe operation. The DØ Cryo control system monitors operation of cooling and dry gas systems, provides additional software interlocks, and provides alarms upon detection of unusual conditions. Both primary and secondary interlocks must be satisfied for a permit to be generated for the application of power to silicon. Temperature sensors on each silicon ladder and wedge assembly provide a third level of over-temperature protection. Over-temperature detected via one of these temperature sensors results in automatic removal of power from the silicon readout HDI it monitors.

Mechanical piping and vessels of the dry gas and cooling systems were designed and fabricated with proper safety and relief devices so that the monitoring and interlock systems are not relied upon for personnel safety. All electrical loads have proper overload protection. The Silicon Detector power system has an extensive *internal* interlock protection scheme provided by its power supply and processor control and data acquisition electronics. Thirty RTD temperature sensors were installed throughout the VLPC fiber barrel structure in order to track the fiber barrel temperatures as the Silicon system is cooled and its purge air flows are adjusted. Those thirty temperature sensors are displayed on the silicon computer graphics pictures.

All interlock design and wiring practices use “failsafe” methods. That is a device must have positive feedback to its electronic circuits or it is considered “tripped”. For example, a normally closed contact would be used on temperature switch in the field. This allows for a lost signal or a disconnected field device to generate a tripped condition. Discriminator modules are used in this system in order to convert an analog value into a discrete signal. These modules are all configured in their failsafe mode, which allows for loss of signal or transmitter failure to result in a tripped condition.

There is one exception to the failsafe practice in the Silicon Cooling System design. That is the control of the cooling circuit in the chiller cabinets. The chiller cooling control is called the Hot Bypass valve, when this valve is energized the chiller is not cooling. If the control signal were lost, the chiller would be forced into the cooling mode, since a solid-state relay is used to control this circuit. This scenario has been countered by using this same DC control voltage that controls the Hot Bypass control, to control the main chiller power solid-state relay. Therefore, if the DC control voltage were lost for any reason the entire chiller would shutdown.

DØ has backup electrical power provided by a diesel generator that starts automatically upon commercial power loss. The Silicon purge air compressors, the Silicon chiller cabinets, and the Uninterruptible Power Supply (UPS) that supplies power to the Silicon cooling system control system are all on backup power. The silicon cooling system monitoring and interlock systems are powered by a UPS, which prevents power interruption to those control systems.

4.5.4 Process control system

The current process control system is based on a number of commercial Siemens Programmable Logic Controllers (PLC’s) and is commonly referred to as the CRYO control system. These

PLC's are capable of handling thousands of physical I/O through remote I/O bases. These remote I/O bases can have many types of modules installed in any of the slots for handling different types of field I/O. These PLC's are commercial computers that have many prewritten communication drivers available. Programming the PLC's is also done through commercial software.

The operator interface is based on the commercial distributed control platform of Intellutions FIX32. FIX32 provides computer alarms, graphical pictures with real time values, operator security, and historical collection of data. Fermilab's use of FIX32 originated at DØ and it is now commonly used throughout the Lab.

The Cryo Control System monitors and controls the Helium Refrigerator, LAR Calorimeters Cryo, Super conducting Solenoid cryo, Instrument Air, Vacuum, Building HVAC, WAMUS and Solenoid magnet power supplies, and the VLPC cryo.

The Cryo control system was expanded with the addition of I/O base eleven on the South sidewalk and I/O bases seven, eight, and ten on the detector platform in order to pickup the physical field devices for the Silicon cooling system and dry purge air system. The Silicon cooling system and dry purge air system logic programming were added to the PLC that has plenty of program capacity. The Silicon cooling system and dry purge air system computer graphical pictures and database blocks were developed and added to the FIX32 system.

The Silicon cooling system may run attended or unattended by operators. The alarms have been picked, programmed, and configured to be consistent with the other systems that the control system runs and monitors.

DØ incorporates a layered alarm strategy. There are typically three layers of alarms. The first is a computer alarm that notes when a parameter is slightly out of normal tolerance. The second is a computer alarm when a parameter is more than slightly out of tolerance. The third is an Auto-Dialer alarm when the parameter is at a point where immediate attention is necessary.

Computer alarms are generated via the FIX32 software. A computer alarm can be routed and filtered by any of many FIX32 nodes throughout DØ and Fermilab. When a computer alarm occurs, all the FIX32 nodes that are set up to filter in the alarm area of a particular alarm will start beeping. This beeping will continue until the alarm condition is cleared and the alarm is acknowledged. An operator with the correct security privileges may set the alarm thresholds and also acknowledge these alarms.

The Auto-Dialer alarm is generated by the PLC and a computer dedicated to running a software package called WIN911. This software package is capable of paging people's pagers with a numeric code as well as calling inside and outside the lab using the telephone system with a voice-synthesized message. The Auto-Dialer is preprogrammed with a list of "experts" who can deal with the particular systems' problem that created the alarm. The Auto-Dialer will continue paging and calling people serially on this list until someone acknowledges the alarm or the alarm condition ceases. The Auto-Dialer is what really makes unattended operation practical at DØ.

5 READOUT ELECTRONICS

5.1 Overview

The readout system for the Layer 0 silicon detector will be based on the new SVX4 readout chip and the existing Run IIa silicon data acquisition system. Sensors are connected to the outside world through hybrids with the SVX4 chips, and an external path consisting in turn of low mass jumper cables, junction cards, twisted-pair cables, adapter cards, and high mass cables followed by Interface Boards, Sequencers and VME Readout Buffers. A brief overview of the main ingredients of the readout system is presented in this section. Conservative solutions allowing for the fastest implementation of necessary changes were favored among different design options.

The SVX4 chip, designed as a joint DØ and CDF project, will be able to function in SVX2 mode and, therefore, should be compatible with the Run IIa readout electronics as discussed in detail in the next section. The chips will be mounted on hybrids. The innermost layer requires a substantially different design due to its very small radius and stringent requirements on the amount of material. For this layer, low mass analog readout cables will couple the silicon and hybrids as shown in Figure 39. This allows the hybrids and silicon to be mounted independently, moving the mass and heat load of the hybrids out of the active detector volume. One 2-chip hybrid reads out one silicon sensor. To minimize the length of the analog cables between different sensors, the sensor closest to Z = 0 is connected to the closest hybrid. Digital jumper cables connect the hybrids to Junction Cards. While the added capacitance from the flex cable degrades the signal-to-noise (S/N) ratio, we expect to achieve a S/N>10 for the SVX4 with analog cable readout even after irradiation as was explained in Section 3.2. Section 5.3 discusses issues related to the analog cables.

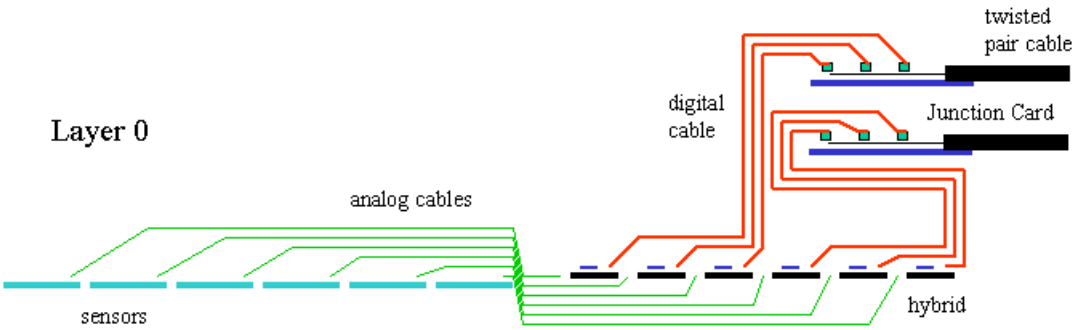

Figure 39 - Concept of readout for Run IIb Layer 0 (with six sensors).

The total readout cable count for Layer 0 is 48.

A major consideration in the design has been to preserve as much of the existing Run IIa silicon data acquisition system as possible and to reuse the associated cable plant. Nevertheless, a few modifications are necessary to address two important issues:

1. The SVX4, produced in 0.25 μm technology will require lower operational voltage, 2.5 V as compared to 5 V necessary for SVX2. The allowed operational range of 2.25 to 2.75 V for SVX4 poses significant restrictions on the voltage drop in the power lines.

2. Modification of control signals are needed to accommodate the difference between the SVX2 chip and the SVX4 chip operating in SVX2 mode.

Figure 40 shows a block diagram of the Run IIa silicon data acquisition. SVX2 chips are read out with approximately 2.5 meter long low mass cables to the passive Adapter Cards located on the face of the calorimeter (Horseshoe). Interface Boards are connected to the Adaptor Cards with 6 meter long 80 conductor cables and serve as distributors of low voltages, bias voltages, data and control sequences for the detector. Interface Boards also monitor the temperatures and low voltages. Sequencers on the Platform provide clock and control signals for the SVX2 chips. The sequencers are also used to read out data from the chips and send that data to the VME Readout Buffers via optical fibers. The hardware components for the Layer 0 readout system are expected to remain the same as used in Run IIa with the exception of those parts highlighted in gray. Adapter Cards and Low Mass Cables will be replaced with new components. Some firmware modifications in the sequencers will also be required as discussed in Section 5.6.

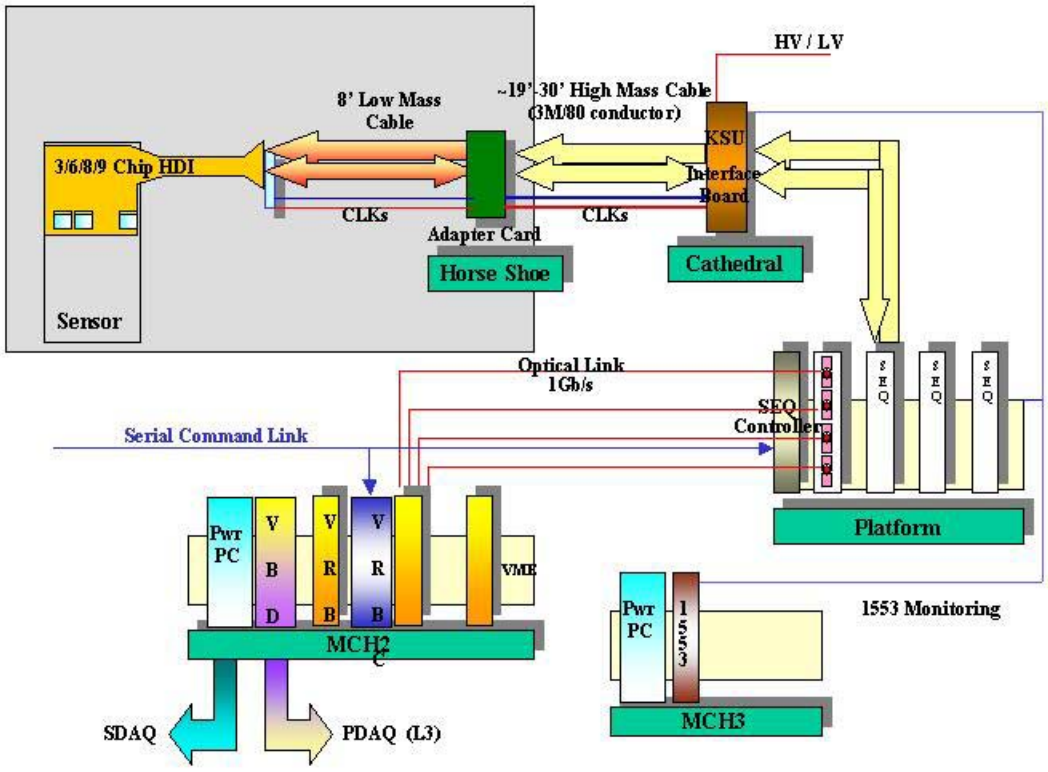

Figure 40 - Block diagram of the Run IIa silicon data acquisition system.

Figure 41 - Block Diagram of the new components of the Layer 0 data acquisition system. shows the block diagram of the new components for the Layer 0 data acquisition system. The Run IIa philosophy, having each hybrid connected to a single Interface Board channel, is preserved. However, the segmentation of this connection and the functionality of the intermediate pieces is different from that in Run IIa. A short low mass jumper cable starts from the hybrid and is routed to the H disk region where a passive junction card is located. The junction card is connected to a new Adapter Card via a 2.4 meter long twisted pair cable. Data lines are driven differentially from SVX4 chips to the Adapter Card in contrast to the Run IIa approach that has single ended readout. Downstream of the Adapter Card, the lines are single ended.

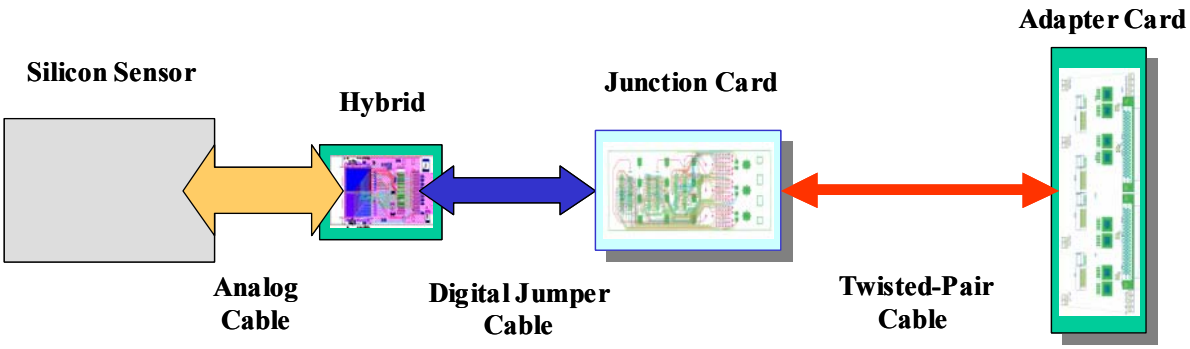

Figure 41 - Block Diagram of the new components of the Layer 0 data acquisition system.

The Adapter Card is a key new component of the data acquisition system accommodating most of the necessary modifications. It will perform the voltage regulation and will contain simple logic for the SVX4/SVX2 conversion as explained in Section 5.5.4. The Adapter Card is connected to the Interface Board with the existing 80-conductor cable. Some changes required for the Interface Boards are described in Section 5.5.5. Sections 5.5.1, 5.5.2, and 5.5.3 contain information about low mass Jumper Cables, Junction Cards and Twisted-Pair Cables. Sections 5.7 and 5.8 have a discussion about low voltage and high voltage supplies and distribution. Results of simulations related to the readout performance are presented in Section 5.9. Grounding issues are discussed in Section 5.10.

5.2 SVX4 Readout Chip

The readout of the detector is accomplished via the SVX4 readout chip, which has been successfully prototyped. The SVX4 is the last of a series of chips developed for silicon sensor readout by the FNAL-LBL collaboration. Earlier versions of such chips were the SVX-B and SVX-H (used in the readout of the first silicon vertex detectors of CDF), the SVX2 (used in the present DØ detector), and the SVX3 (used in the present CDF vertex detector). The SVX4 design thus draws heavily upon the experience gained from these earlier efforts and incorporates many of the desired features gleaned from this experience.

The SVX4 has 128 inputs with a 48 μm pitch, which receive the charge generated by 128 strips of a silicon detector. The input charge, for a well-defined period of time corresponding to a single beam crossing, is integrated and deposited in a capacitor of a switch-capacitor array called the pipeline. This pipeline has 46 cells, of which 42 can be used to store the charge, thus allowing the successive storage of the charge generated during 42 successive beam crossings. If an event is accepted by the Level 1 trigger framework during any one of the 42 beam crossings, the charge of the appropriate capacitor is digitized by an on chip ADC, and the resulting digitized data is sent to the data acquisition system. The data can be read in a read-all mode (*i.e.* in its totality), in a sparsification mode (*i.e.* only channels above a certain threshold value), or in a sparsification mode with neighbors (*i.e.* in addition to the channels above threshold the channels flanking them are also read out). The chip also has a deadtimeless feature, which allows for the concurrent acquisition of charge by the integrators and the pipeline while digitization or readout is taking place; this feature, which is the salient difference between SVX2

and SVX4, will not be used by DØ. Another difference between SVX2 and SVX3 is that SVX3 has the dynamic pedestal subtraction capability, in which the gray code counter in the ADC is forced to start when the number of channels with the comparator firing reaches a preset value. By adjusting the preset value to an appropriate number, it effectively removes the average pedestal over the channels, resulting in an increase of dynamic range and compensation for possible pedestal drift in time. The SVX4 inherits this dynamic pedestal subtraction capability.

Because the SVX4 chip is based upon the SVX3 chip used in the present CDF detector, it incorporates features that were not available in the SVX2 and are not part of the control and readout configuration of the Run IIa silicon data acquisition system. These features have to do mostly with the deadtimeless operation mode of the SVX3, which requires additional control lines and a dual clock (front end and back end clocks). However, it turned out that remapping our control lines to the ones required for the SVX3, which channels our clock to either the front end or the back end clock depending on the mode of operation of the chip, was adequate to operate the SVX3. A test board consisting of a single FPGA and simple transceivers was able to perform the required task, *i.e.* an SVX3 chip was read by the DØ sequencer board, as seen in Figure 42.

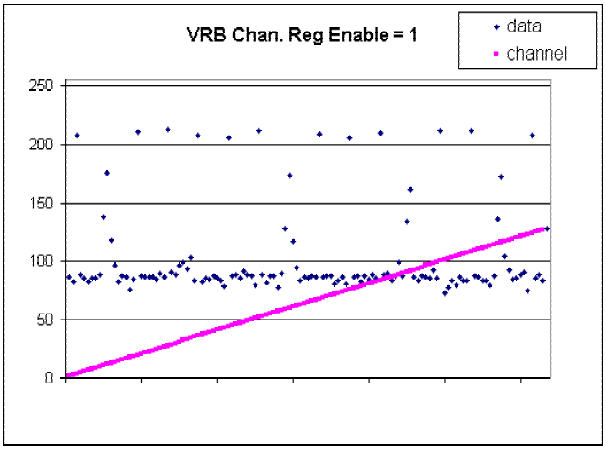

Figure 42 - SVX3 chip performing in SVX2 mode with the DØ data acquisition system (November 2000).

As a result of this successful demonstration, DØ adopted the SVX4 chip designed by a FNAL-LBL-Padova team of engineers and has played an active and significant role in the design effort. The required remapping is shown in Table 10.

Table 10 - Mapping between SVX2 and SVX4 readout/control lines.

SVX 2				***SVX4***			
Mode				Mode			
INIT	ACQ	DIG	READ	INIT	ACQ	DIG	READ
BUS 0 PA RESET	BUS 0 PA RESET	BUS 0 PA RESET	Data 0	BUS4 PARST	BUS4 PARST	BUS4 PARST	Data4
BUS1 RREF-SEL	NC	HIGH	Data 1	BUS3 RREF-SEL	BUS3 RREF-SEL	BUS3 RREF-SEL	Data3
BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	Data2	BUS5 L1A	BUS5 L1A	BUS5 L1A	Data5
BUS 3 PIPE SREF	BUS 3 PIPE SREF	BUS 3 PIPE SREF	Data 3	BUS 6 PRD1	BUS 6 PRD1	BUS 6 PRD1	Data 6
BUS4 CNTR RESET	BUS4 CNTR RESET	BUS4 CNTR RESET	Data4	BUS2 PRD2	BUS2 PRD2	BUS2 PRD2	Data2
BUS5 RAMP RESET	BUS5 RAMP RESET	BUS5 RAMP RESET	Data5	BUS 1 RAMP RESET	BUS 1 RAMP RESET	BUS 1 RAMP RESET	Data1
BUS6 COMP RESET	BUS6 COMP RESET	BUS6 COMP RESET	Data6	BUS0 COMP RESET	BUS0 COMP RESET	BUS0 COMP RESET	Data0
BUS7 SR LOAD	BUS7 CAL INJECT	BUS7 N/C	Data7	BUS 7 CAL/SR	BUS 7 CAL/SR	BUS 7	Data7
MODE0	MODE0	MODE0	MODE0	FEMOD	FEMOD	FEMOD	FEMOD
MODE1	MODE1	MODE1	MODE1	BEMOD	BEMOD	BEMOD	BEMOD
CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE
TN	TN	TN	TN	TN	TN	TN	TN
BN	BN	BN	BN	BN	BN	BN	BN
CLK	CLK	CLK	CLK	FECLK	FECLK	BECLK	BECLK
CLKB	CLKB	CLKB	CLKB	FECLKBAR	FECLKBAR	BECLKBAR	BECLKBAR
DATA VALID	DATA VALID	DATA VALID	DATA VALID	OBDV	OBDV	OBDV	OBDV
PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN
PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT

This modification of control configuration can be accommodated by the existing DØ Sequencer readout module. In addition, the use of internal circuitry of the SVX4 allows the chip to operate in the so-called DØ mode. The circuitry can be turned on via an external wire bond to the digital voltage line. For operation in the CDF mode the wire bond must be connected to ground. In the DØ mode, using internal gating, the clock is sent to the appropriate section (front/back end) depending on the chip's internal mode. The same selector also forces the chip to use the PRD1, PRD2, L1A, and CALSR as inputs from the bi-directional differential data bus (for DØ) rather than their single ended dedicated input pads (for CDF). Thus, to use the existing DØ readout

sequencers the only major change required is a new adapter card with transceivers that will adapt the single-ended 5 V signals used by the sequencer to differential 2.5 V signals used by the SVX4.

The SVX4 readout chip is produced using a deep submicron process (0.25 μm) by TSMC (Taiwan Semiconductor Manufacturing Corporation). Such submicron processing leads to a very small oxide layer that in turn results in a highly radiation tolerant device, without having to resort to any special manufacturing processing. Chips developed in such a process (such as the APV25 chip for the CMS experiment and the VA1 chip for the Belle experiment) have been subjected to radiation doses exceeding 20 Mrad with no sign of radiation damage, and will survive the expected doses for our detector. These submicron process chips require a power supply of +2.5 V, as opposed to the +5 V and +3.5 V of the existing SVX2.

In order to test and characterize the prototype chip in various aspects, we used three different test setups. The first setup at LBL is based on a pattern generator controlled by a Linux computer. In simplest terms this setup consists of two FIFOs, a clock oscillator, and an interface board to the computer. It is simple, flexible, well suited for quick extensive tests requiring frequent changes of download parameters and control sequences. However, the LBL setup does not allow clock frequency above 35MHz while the operational frequency is 53 MHz. The second setup is located at Fermilab, consisting of a sophisticated pattern generator with fine adjustment of timing (stimulus machine) controlled by a computer. Because of the capabilities of the stimulus machine, this setup has an advantage in detailed timing, frequency, and duty cycle studies. Most importantly this setup is capable of running at up to 100 MHz clock frequency. The two setups above, therefore, are very much complementary. Detailed description of the stimulus setup and tests performed with the setup is available in Section 5.2.1. The third setup used for testing of SVX4 behavior on hybrids is based on the Standalone Sequencer and Purple Card. This setup is described in detail in Section 6.

Wafers of SVX4 chips will also be tested by R.Yarema's group at Fermilab prior to dicing.

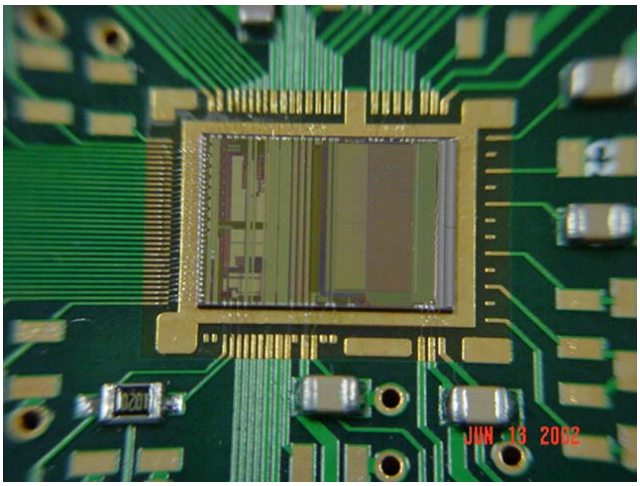

Figure 43 - A photograph of the prototype SVX4 chip mounted on chip carrier board.

The first prototype chips were fabricated, and delivered to Fermilab and LBL in June 2002. Figure 43 shows the first prototype mounted on a chip carrier board in the LBL test setup. Since then, extensive tests have been performed using the three setups described above, as well as independent measurements of the front-end preamplifier. The most important conclusion is that the tests confirm the full functionality of the chips in both CDF and DØ modes. In the following, we list the highlights of test results.

A preamplifier design with excellent frequency response, good reset time, good power supply noise rejection, and good noise performance has been identified. The overall noise of the analog section, *i.e.* preamp and pipeline combined, has been measured as $[300+41\times C(pF)]e^-$ with 100 ns integration time and 70 ns preamp rise time, where the C is the input load capacitance. The preamp and pipeline gains have been found to be consistent with the specification. Non-linearity including both the analog and digital parts has been measured to be <0.3%. For the ramping voltage in the ADC, the offset level and the ramping rate are in good agreement with expectations for the design. It is confirmed that the data output driver reproduces the input from the daisy chain, and passes the copied signal to the next chip. There are two configuration registers; a serial shift register and a Single Event Upset (SEU) tolerant shadow register. By changing the parameters stored in these registers, all bits have been checked to work as configured. The power consumption has been verified to agree with expectations. The different readout options, such as the sparsification mode, the dynamic pedestal subtraction, and ReadNeighbor feature have been tested.

An important issue to study was the frequency and duty cycle behavior. In the actual detector with a large number of channels, the duty cycle of the clock may be different from the ideal 50% form because of the long transmission lines of various lengths. This requires safety margins for the duty cycle and frequency of the clock

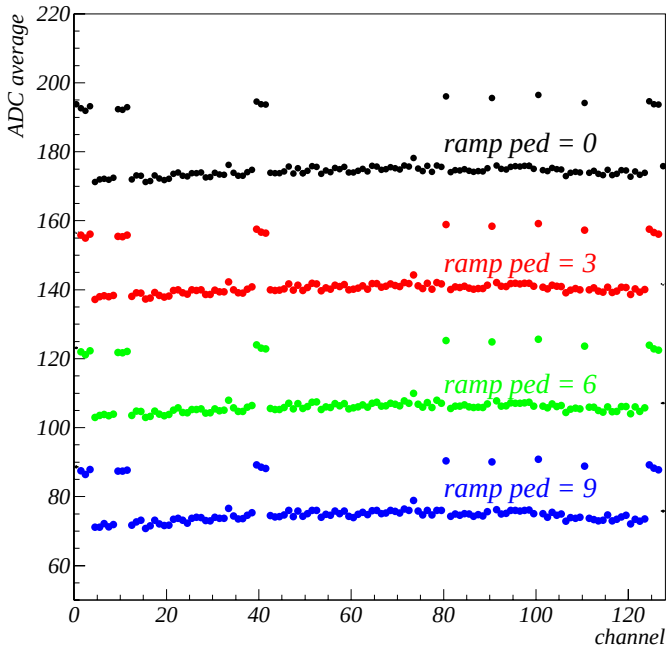

Figure 44 - Average of ADC counts for 100 events across the channels. The calibration charge is injected to the channels with higher ADC counts. The offset of ramping voltage in the ADC has changed, and thus the digitized ADC counts for the calibration charge (= difference between the charged injected channels and the others) is constant.

Figure 44 and Figure 45 show the ADC counts for all 128 channels with some configuration parameter settings. The calibration charge is injected to the channels with higher ADC counts. It is verified that variation of the configuration parameters correctly affects the output ADC counts, as seen in the two figures.

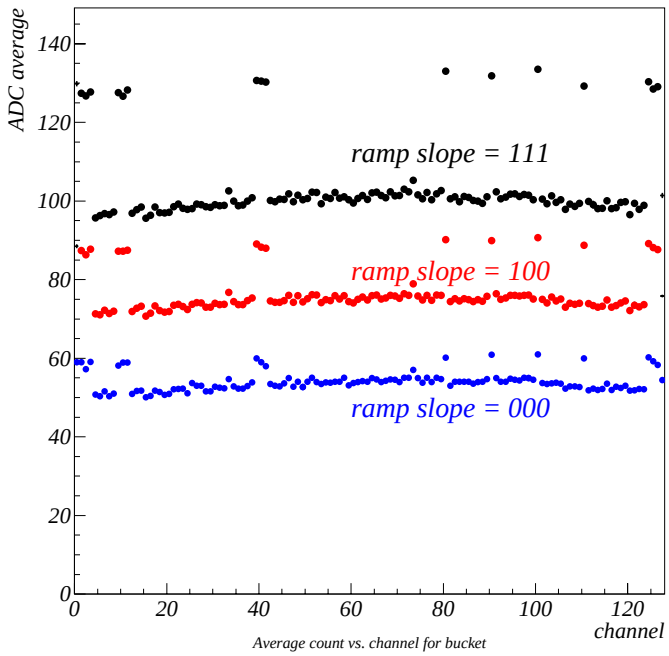

Figure 45 - Average of ADC counts for 100 events across the channels. The calibration charge is injected to the channels with higher ADC counts. The ramping rate in the ADC is varied. This gives the change in both the digitized ADC counts and pedestals.

An irradiation test for the analog front end part had been conducted for the test chip, which consisted of only preamp and the pipeline, using a ^{60}Co gamma ray source. While the test result did not show any significant performance degradation, the prototype SVX4 chip should also be irradiated. We planned two separate studies. The first one is irradiation by hadron beam for testing the shift register and the Single Event Upset (SEU) tolerant shadow register. To check if there are any corrupted bits in the shift register during exposure, the chip will be kept running and shift register values will be read out continuously. The shadow register also has to be examined at the same time. The second test checks sensitivity to total doses. This test uses a ^{60}Co gamma source.

As shown above, no fatal failures or bugs in chip operation were found. However, some undesirable features were revealed. As a result of the detailed studies outlined above, several modifications to the SVX4 design were implemented including modification of the ADC control sequence to facilitate switching between Acquire and Digitize in DØ mode, modifications of two bit assignments in the data field, and layout modifications in the ADC for better pedestal uniformity across the channels. A full pre-production run of 24 wafers of this revised SVX4 chip was submitted in April and received in May of 2003. Results from testing of this chip indicate that the chip is fully functional. The yield appears to be quite high and no undesirable features have been observed. This pre-production run of SVX4 chips will provide sufficient chips to readout the proposed Layer 0 detector.

5.2.1 SVX4 tests with stimulus setup

The stimulus test stand was originally designed for testing the SVX2 silicon readout ASIC and then upgraded for SVX3 prototyping and testing. We have modified this system for SVX4 testing.

The stimulus test stand consists of a PC with a GPIB interface card, a DAC-812 and a PCL-710 digital counter both connected through an ISA port. A custom DAQ program (SVXEval) was written for Windows 9x. The program algorithmically constructs patterns in memory and transmits them via GPIB to a Tektronix HFS 9003 Stimulus System. The PC also programs a HP 16500B Logic Analysis System over GPIB. The PC is a 200 MHz Pentium with 64 MB of RAM and is running Windows 98. We show the entire system in Figure 46.

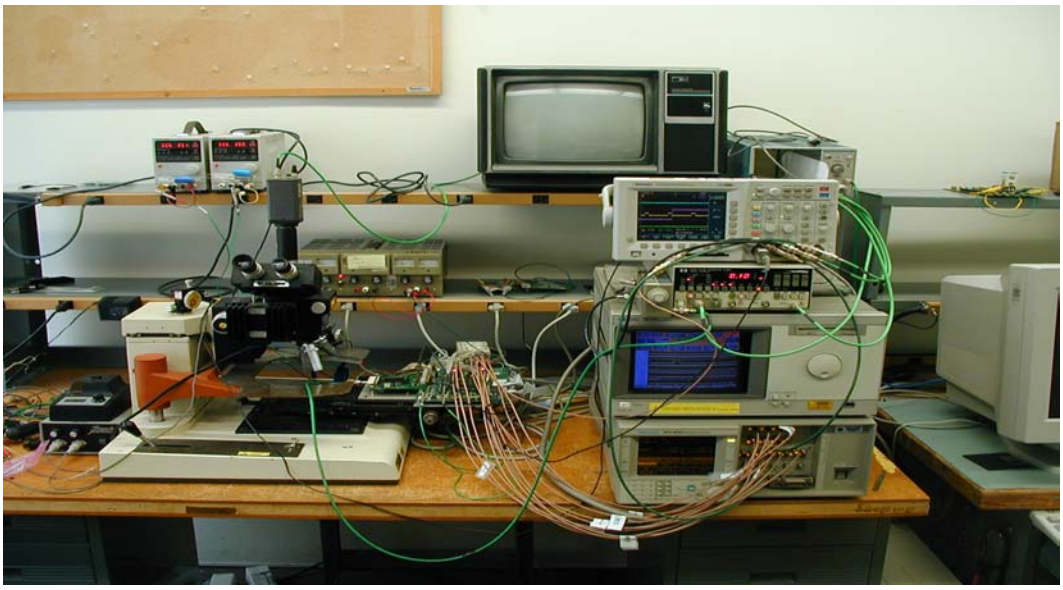

Figure 46 - The Stimulus Test Stand. The PC is located to the far right. The Stimulus System is located next to the PC below the Logic Analysis System, HP Pulse Generator, and Tektronix TDS 3034 Oscilloscope (in order from bottom to top). Cables connect the Stimulus System outputs to the SVX4 Adaptor Board located in the middle which is connected to a SVX4 chip carrier. The Adaptor Board and Chip Carrier are mounted on a movable table of the Rucker & Kolls Probe Station that has a Bausch & Lomb MicroZoom microscope connected to the television. The power supplies for the Adaptor Board and SVX4 chip can be seen as well as the power supply to two Picoprobes that are used to probe pads located on top of the SVX4 chip itself.

The Stimulus System sends patterns to the SVX4 through a custom designed interface board and has a maximum speed of 630 MHz. The frequency for normal operation is 530 MHz which allows an ability to change the waveform at the level of 2 ns. The Stimulus System has a total pattern memory of 64 K vectors which allows a pattern length of 128 μs. In practice, the pattern memory is divided into different cycles of SVX4 operation and these individual patterns can be repeated indefinitely.

The HP 16500B Logic Analysis System contains a 4 GHz/1 GHz Logic Analyzer along with a 2GS 32K Oscilloscope. The Logic Analysis System has two HP pods with flying-lead probe tips

that are used to monitor the signals being sent to the SVX4 chip via the SVX4 adaptor board and the data output from the SVX4 chip. Each pod has 8 data lines which gives us the ability to monitor 16 different signals in the system. One probe is used to monitor control signals and the other is used to view the data from the SVX4 chip. We are able to graphically view the waveform being downloaded to the chip and the data coming from the chip.

The SVX4 Adaptor Board, designed by the University of Kansas, has multiple functions. Because the Stimulus System cannot generate enough control signals, an EPLD located on the Adaptor Board is used to generate the extra control signals necessary for proper SVX4 chip operation. The Adaptor Board properly terminates the signal and bus lines of the SVX4 chip, contains test points which give convenient connection points for the flying-lead probe tips of the Logic Analysis System, and allows for dual mode (DØ/CDF) operation of the SXV4 chip. We show the SVX4 Adaptor Board in Figure 47.

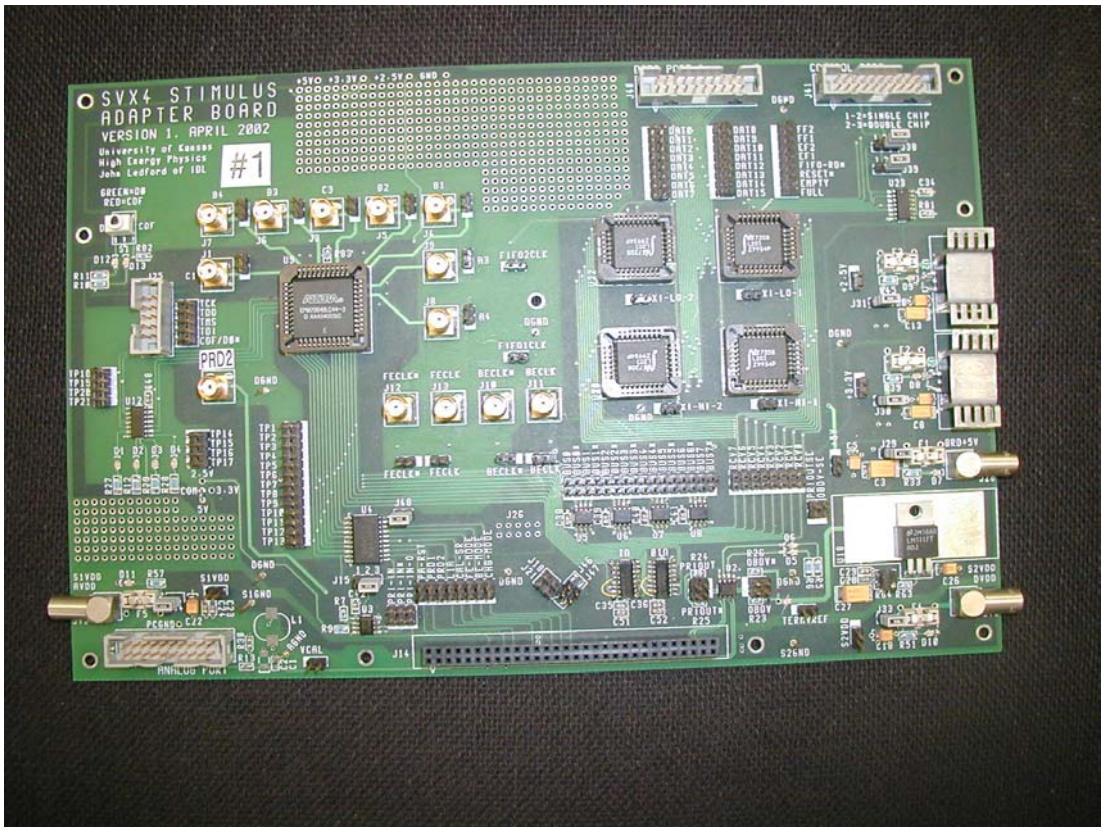

Figure 47 - The SVX4 Adaptor Board. The Adaptor Board is used to interface the Stimulus System with the SVX4 chip. This board contains an Altera EPLD which contains a finite state machine used to generate the extra control signal for proper SVX4 operation. It also contains four FIFOs that are used to buffer data between the chip and the computer. The 60 pin connector in the middle of board is the connection used to the SVX4 chip carrier. The Lemo connectors at the sides of the board are used for power connections.

In Figure 48, we show a cartoon representation of the hardware for the Stimulus Test Stand. The computer sends a pattern to the Stimulus System via the SVX4 Adaptor Board. The SVX4 chip is mounted onto a carrier board. The data from the chip is stored in FIFOs on the Adaptor Board

until the computer can read out the data. The Logic Analyzer has two pods which probe test points on the Adaptor Board and gives a graphical representation of the waveform and the data output of the SVX4 chip.

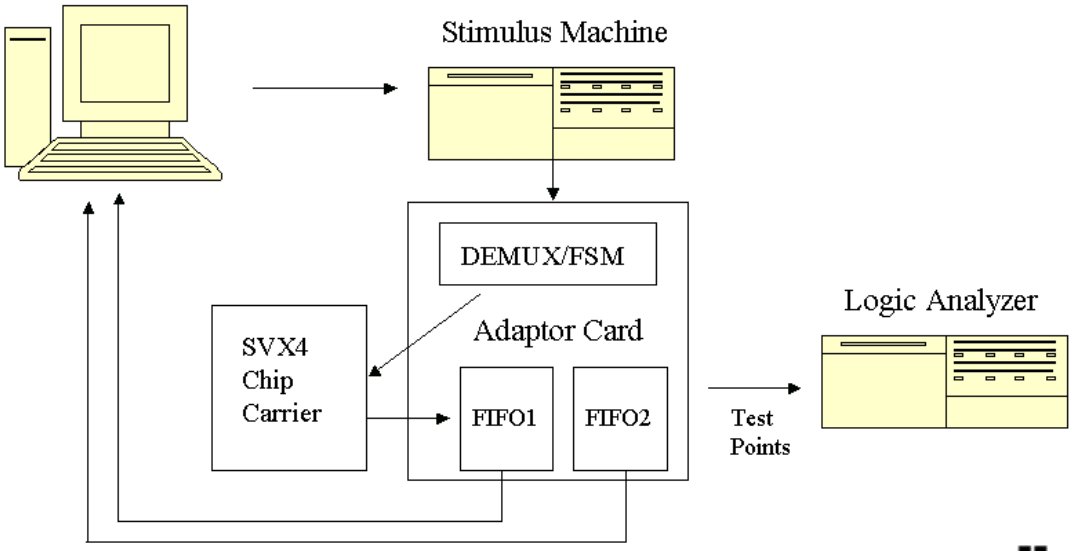

Figure 48 - Cartoon representation of the Stimulus Test Stand. The PC is connected to the Stimulus System and the Logic Analyzer through GPIB. The SVX4 Adaptor Board is in the middle with the demultiplexer/finite state machine (programmed inside the EPLD on the board).

The waveforms that are downloaded to the chip are generated algorithmically and can be altered by a graphical waveform display/editor provided by the software. We show the waveforms for the DØ mode and CDF mode of the SVX4 chip in Figure 49.

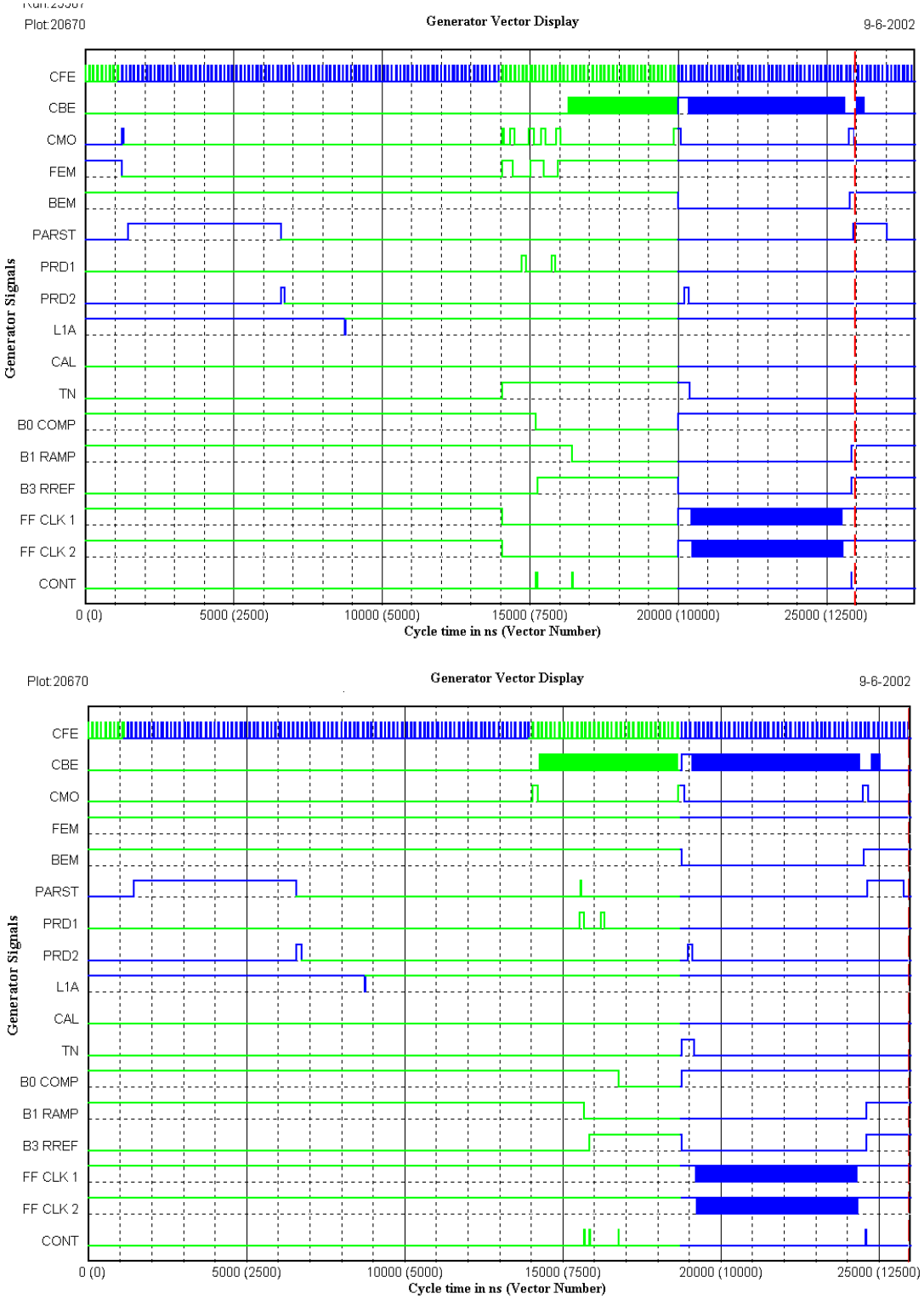

Figure 49 - DØ (upper) and CDF (lower) waveforms. These waveforms are generated algorithmically by the DAQ software and are download to the SVX4 chip via the adaptor board. The three signals corresponding to setup of the ADC (COMP, RAMP, and RREF) are shown here only for understanding the timing. The actual signals are generated by the EPLD by using the control (CONT) signal. The FIFO clocks are no longer used.

The stimulus system is fully operational and the SVX4 performance tests have been completed. An interesting measurement done with this setup is the study of the current consumption of the SVX4 during an entire data cycle (see Figure 50). A data cycle consists of entering the Acquire cycle followed by the Digitization cycle and Readout cycle. We used a calibrated current probe on the individual power supplies (AVDD and DVDD) and then we connected both power supplies together and measured the contribution from both the front-end and back-end from the single supply. This is important because it is necessary to know what the average and peak currents that the power supplies must be able to generate when powering the detector.

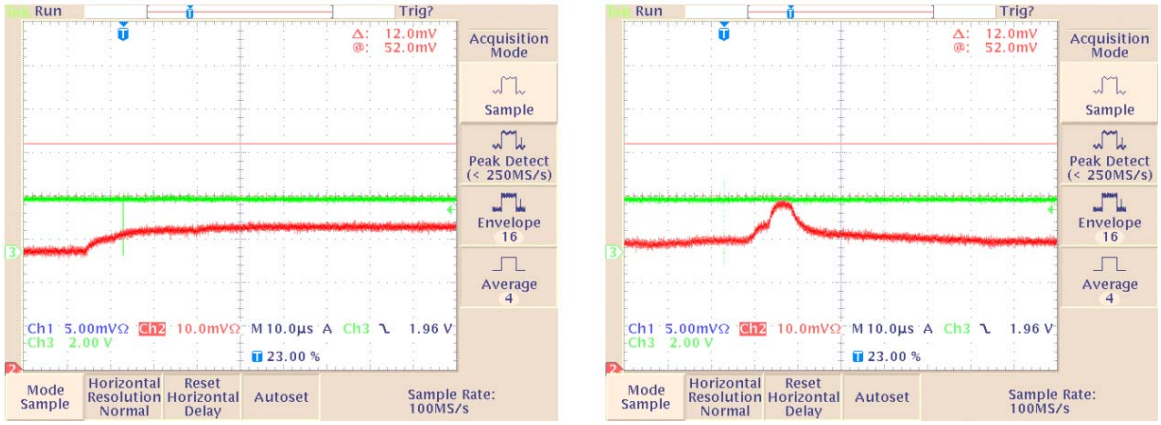

Figure 50 - Current consumption of the SVX4 Version 2 chip. The left hand picture is the current consumption for an independent supply connected to AVDD=2.5 V. The vertical scale is 20 milliamps/division with zero is the lower left corner. The right hand picture is the current consumption of an independent power supply connected to DVDD=2.5 V. The scale is also 20 milliamps/division with zero in the lower left corner.

For consistency we powered AVDD and DVDD from one power supply to measure the combined current draw from the front-end and back-end during one data cycle. This is shown in Figure 51.

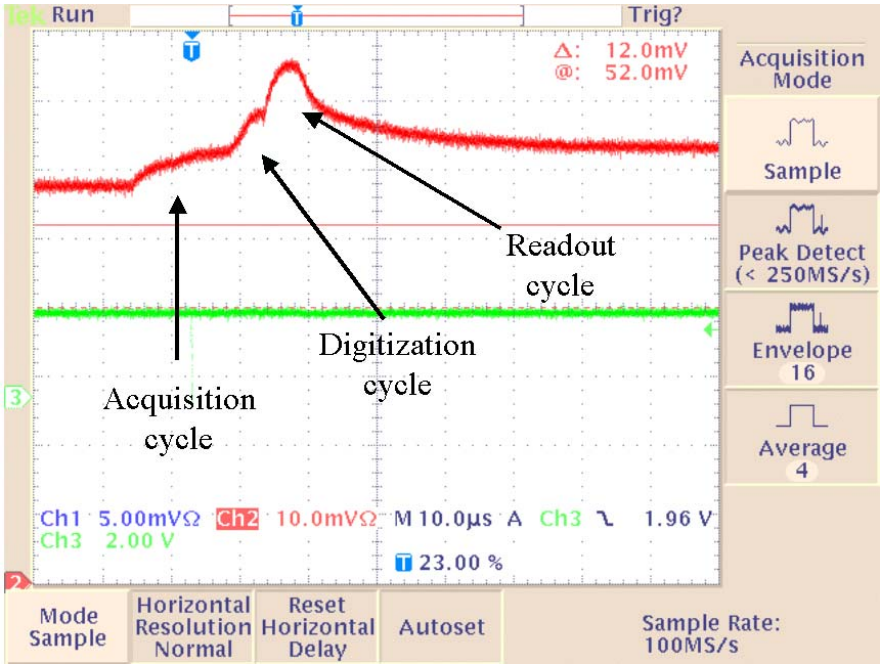

Figure 51 - Current consumption of the SVX4 Version 2 chip. The vertical scale is 20 milliamps/division with zero is the lower left corner. Both AVDD and DVDD are connected to the same power supply: AVDD=DVDD=2.5 V. The scale is also 20 milliamps/division with zero in the lower left corner. The sum of the individual currents sum to the total within a few percent.

5.3 Analog Cables

Analog signals from the silicon sensors are transmitted to the hybrid containing the SVX4 chips by flexible circuits up to 360 mm long with fine-pitch copper traces. While very attractive because of material and heat eliminated from the sensitive tacking volume, this approach represents a considerable technical challenge. The addition of the analog cable deteriorates the noise performance of the silicon sensors. Procurement of the flex cables and the complicated module assembly are other non-trivial issues. Nevertheless, a similar design is used by CDF for the readout of the innermost layer L00 in the Run IIa SVX detector, and several prototypes were fabricated and successfully tested for L0 of the DØ Run IIb detector.

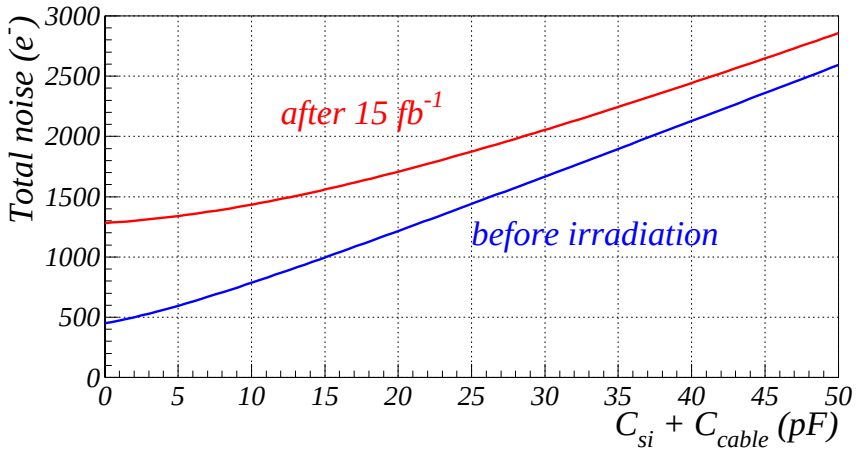

Figure 52 - Expectation for the total noise as a function of sum of sensor and cable capacitance.

One of the most important aspects in the design and technical realization of a long analog cable is the capacitance between the traces, which should be as small as possible. Any load capacitance will contribute to the noise seen by the preamplifier. Our design goal is to maintain a S/N ratio of better than 10 for Layer 0 after irradiation. Figure 52 shows the expected noise level as a function of capacitance summed over silicon sensor and analog cable. Assuming that a minimum ionizing particle creates 22,000 electrons by traveling through a silicon sensor with the thickness of 300 μm, the total capacitance must be kept below 33 pF to maintain the S/N better than 10 given the measured SVX4 noise performance. A 12 cm long silicon sensor will have about 15 pF of capacitance. This means that the analog cable is required to have capacitance less than 18 pF or 0.5 pF/cm.

The flexible dielectric substrate of the cable affects the capacitance. The material of choice in high-energy applications is polyimide such as Kapton HN with a dielectric constant of 3.5 at a frequency of 1 MHz. This material is radiation hard with good mechanical and electrical properties. Other synthesized polyimide materials on the market achieve a lower dielectric constant by adding halogens. They are not radiation hard and are not in compliance with CERN and Fermilab fire safety regulations. Although materials such as polyethylene or polypropylenes are used in the flex circuit industry and provide a lower dielectric constant, they are also not radiation hard up to the 10 to 15 MRad level, to which the innermost layer of the silicon tracker may be exposed. The material choices for the flex cable are, therefore, limited to the standard polyimide.

Considering the tight schedule and the technical difficulties, we investigated a design that allows a manufacturer to produce cables reliably, and also satisfies the capacitance requirement.

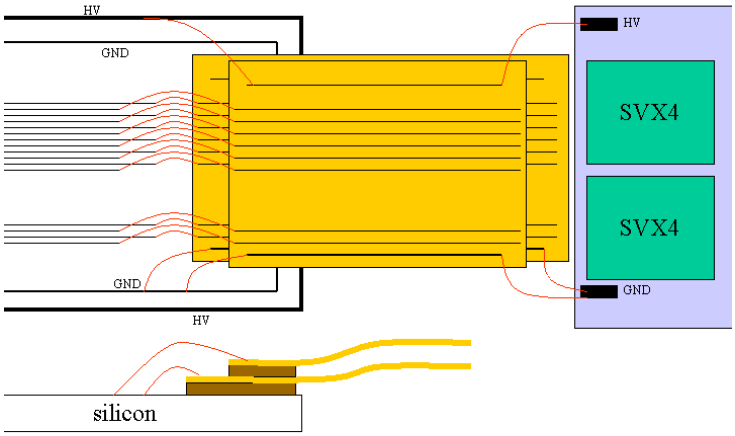

Figure 53 - Schematic view of the proposed connections between the sensor, analog cable and the hybrid for Layer 0.

Figure 53 shows a schematic view of the arrangement for the sensor, analog cable and the hybrid for Run IIb layer 0. Two cables with constant 91 μm pitch are laminated together with a lateral shift of 45 μm. This works effectively as a cable with 45 μm pitch. We believe this is a simpler alternative to the L00 approach that has fan-in and fan-out regions adapting the 45 μm pitch to 100 μm pitch. We also investigated the dependence of the cable capacitance on the trace width to understand the trade-off between the reliability and performance.

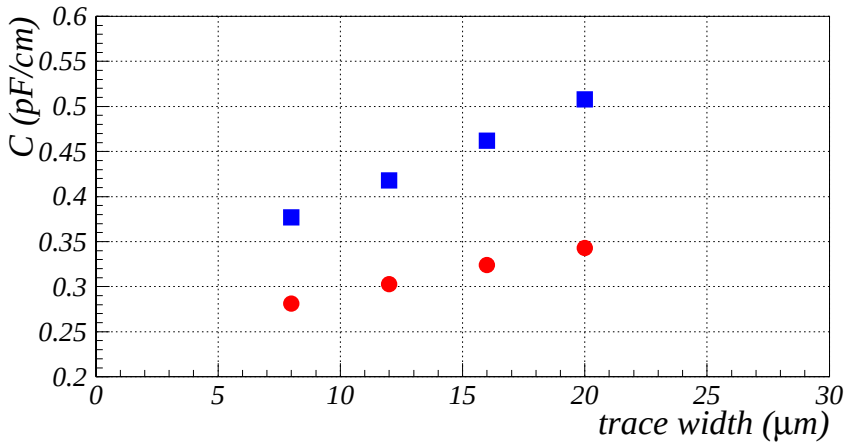

Figure 54 - Capacitance calculations by ANSYS. The capacitance of one trace to all other traces is shown as a function of trace width. The blue squares represent 50 μm trace pitch, and red circles 100 μm.

Figure 54 shows the expected capacitance for various trace width and different pitch by finite element calculations using the ANSYS program. The height of the traces is assumed to be 8 μm in the calculations. It turns out that the 100 μm pitch cable reduces the capacitance by 30% compared to the 50 μm pitch. Besides, the dependence on the trace width is weaker for the 100 μm pitch, correspondingly 0.0052 pF/cm/μm for the 100 μm pitch and 0.0109 pF/cm/μm for the 50 μm pitch. Based on this result of the calculations, we adopted the following design as a baseline for Run IIb layer 0 analog cables: 16 μm trace width and 91 μm constant pitch with no fan-in/out region. The 16 μm trace width is a factor of two larger than the trace width of the L00 CDF cable, which we expect to result in increased reliability and higher production yield of the cable. In the final design of the Run IIb analog cables, the pitch is reduced from 100 to 91 μm because the HV trace was expected to hold up to ~1000 V and, therefore, needed to be separated by more space on the cable.

In order to reduce the capacitance contribution from adjacent cables, a spacer is placed between the cables. A candidate for the spacer material is polyimide mesh sheet with dielectric constant 3.5. The effective dielectric constant of the polyimide mesh can reduced by removing more material from the mesh. Prototypes of this mesh have been fabricated by using a laser to cut material from a polyimide sheet, as shown Figure 55. The thickness of the Run IIb spacer was to be 200 μm at maximum because of mechanical constraints. The capacitances calculated by ANSYS for this configuration with two cables and a spacer are summarized in Table 11.

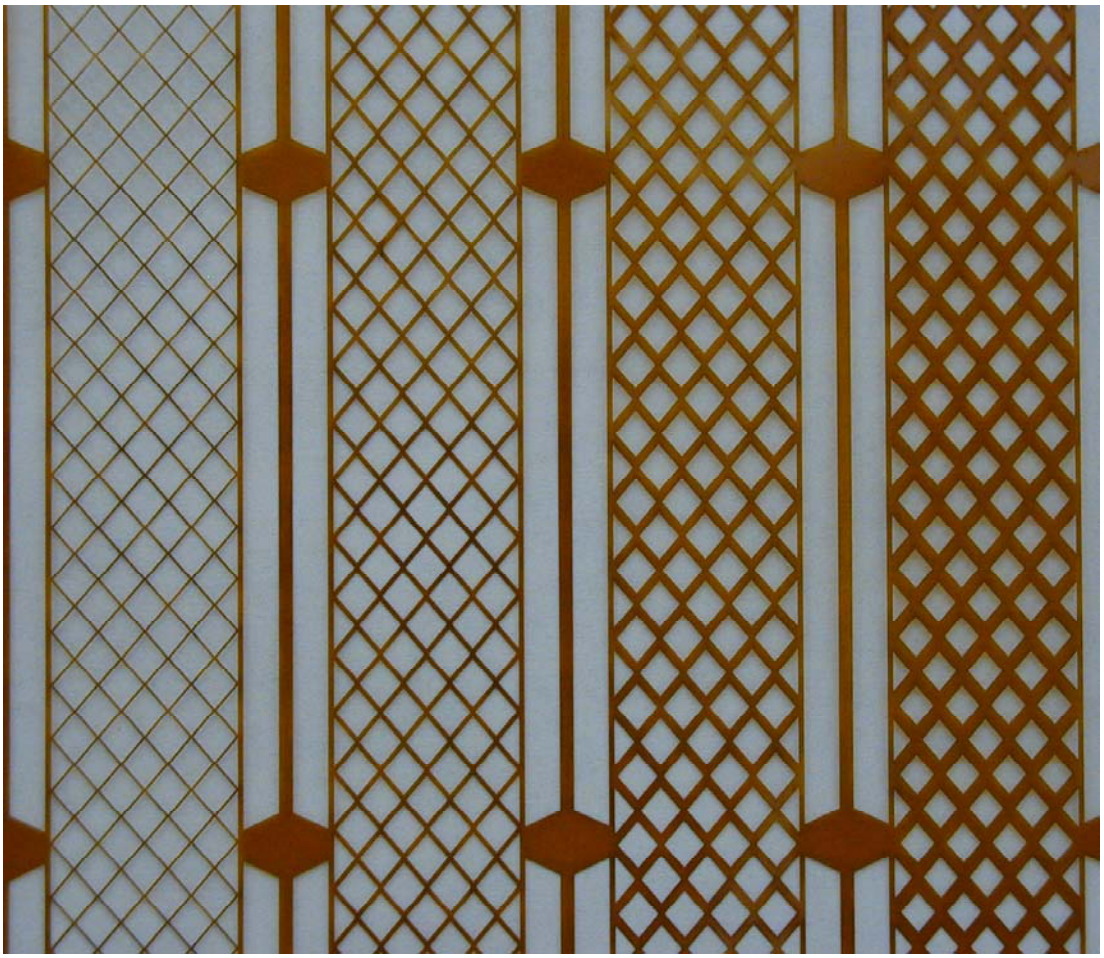

Figure 55 - Photograph of several different density Kapton meshes made as spacers for analog cables.

Table 11 - Capacitance of one trace relative to all other traces calculated by ANSYS. The first line is for a single cable, and the other for the configuration where two cables are laminated together with the 200 μm thick spacer. The first column is the dielectric constant for the spacer.

ε_r of spacer	Capacitance (pF/cm)
Single cable	0.339
1	0.342
2	0.466
3	0.585

This result indicates that separating two cables by a proper spacer can maintain cable capacitance below the required value. From this encouraging result, DØ adopted the method of using two 91 μm pitch cables for one chip readout, in which a pair of cables with a spacer functions as a 45 μm pitch cable for Run IIb layer 0. This technique allows the trace pitch to be almost twice that of the SVX4 bond pads, resulting in relief of the technical difficulty of fabricating such a fine pitch flex circuit.

Based on good prior experience with high density interconnects (HDI) from Dyconex Inc. in Zurich, Switzerland, we contacted them in May 2001. After a few iterations of their prototyping and our technical evaluation, in July 2002 they delivered 27 good prototypes. Figure 56 is a photograph of one of the prototype Run IIb analog cables. The copper traces are gold-plated, and the bonding pads have been confirmed to be bondable. Out of the 27 cables, 25 cables satisfy the specification in the number of open traces. While the specification is that 128 traces out of 129 (one trace is spare) are continuous, 16 cables have no opens, and 9 cables have 1 open. Another important requirement is capacitance. The specification is <0.40 pF/cm. The capacitance of one trace to neighboring two traces was measured to be 0.30 pF/cm. From ANSYS calculations, a 10 to 15% increase is expected from contributions besides the two neighbors. Measurements on an old prototype cable with all the traces were shorted together had verified this increase rate. Therefore, 0.35 pF/cm is a fair estimate of the capacitance. This is within the specification.

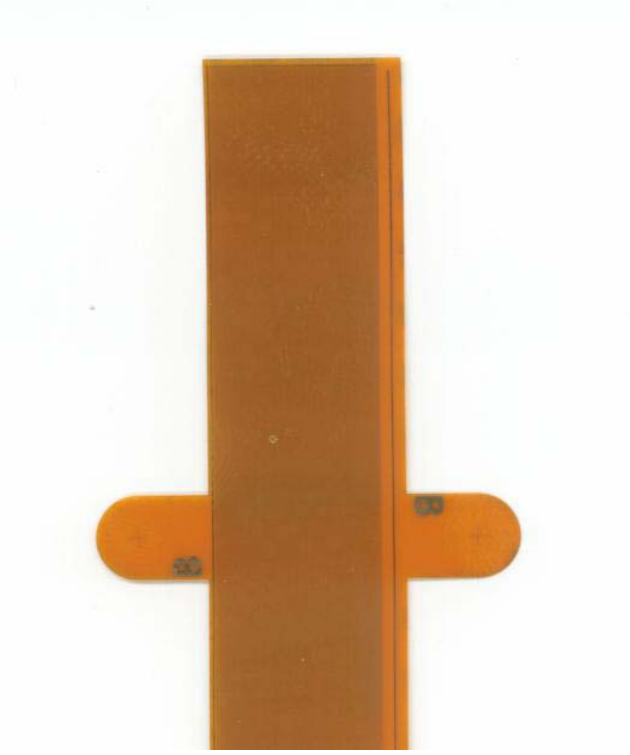

Figure 56 - Photograph showing the edge of a recent prototype Run IIb analog cable.

We anticipate that the design of the analog cables for the proposed Layer 0 detector will be based upon the successful Run IIb prototypes. Note, however, that the end of the analog cable that is to

be bonded to the sensor will likely include an integrated pitch adapter to match the sensor readout strip pitch, and the thickness of the spacers may need to be reduced to ≈150 μm due to the tight space constraints associated with this detector.

5.3.1 Measurements using Run IIb Layer 0 prototype analog cables

In Layer 0, the tight space constraints and heat dissipation issues lead us to use a low-mass analog cable to couple the silicon sensor and the SVX4 chip mounted on the hybrid. As discussed in Section 5.3, special attention has to be paid to the capacitance increase caused by the long analog cable, to avoid degradation of the noise performance. In addition, the experience of the Run IIa L00 in CDF reveals other possible noise sources: noise due to capacitive coupling between the detector and nearby floating metal such as cooling tubes, and also RF pickup noise by the analog cable.

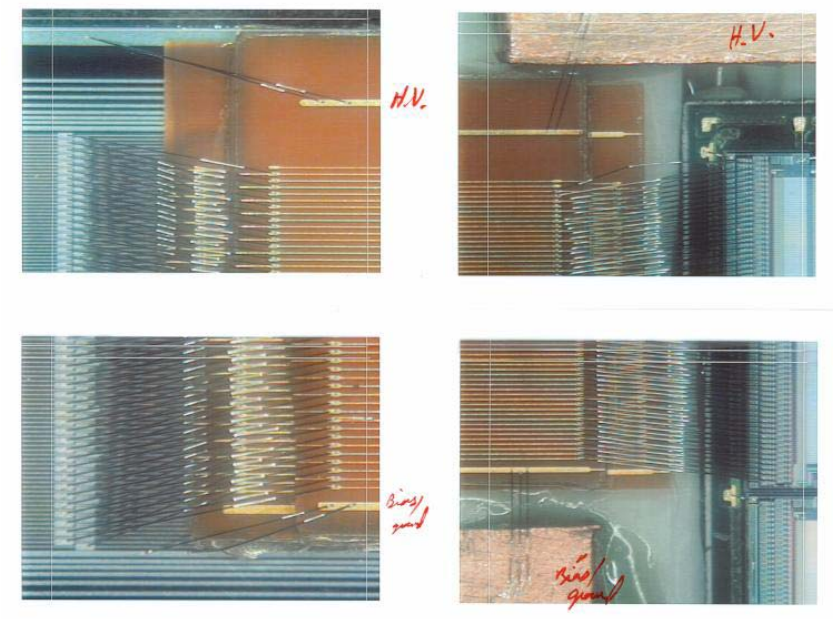

Figure 57 - The photograph of the connected region between the sensor and the analog cable (left) and between the cable and the chip (right).

In order to study the effect of these additional noise sources, a L0 prototype was assembled from a Run IIb L0 prototype sensor manufactured by ELMA, an analog cable manufactured by Dyconex, and a Run IIa hybrid for the readout. The wire-bonding regions for the sensor to the analog cable and for the cable to the chip are displayed in displayed in Figure 57. The L0 prototype fixture is put inside a plastic box for light tightness, and is well insulated to avoid any capacitive coupling to the assembly. There are three SVX2 readout chips mounted on the hybrid. Out of the three, two are used to read out the signal from the sensor through the analog cable, while the remaining chip does not have any input loads, and serves as a reference noise level in the test setup. In the noise study described in this section, the noise level is defined as the RMS of pedestal distributions for 100 events.

Apart from the electrical measurements described below, this prototype is a successful demonstration of the proposed arrangement for analog cables. The prototype allowed us to come up with specifications on exact dimensions for the final system and to verify the feasibility of bonding between the cables and the sensor and between the cables and the hybrid.

First we measure the noise level in an electrically quiet environment (accomplished by wrapping the whole fixture by aluminum foil connected to ground), to estimate the amount of additional noise due to the load capacitance of the analog cable. The left plot in Figure 58 shows the noise level for each channel. The projection in each chip is shown on the right. From Gaussian fits of the distributions, the average noise level is 2.2 ADC counts, compared to 1.4 ADC counts in the third (reference) chip. Assuming one ADC count is equivalent to 1000 electrons, the increase of noise level can be translated as 800 electrons. Using the fact that a minimum ionizing particle creates roughly 22,000 electrons in a sensor, the observed noise from the additional capacitive load is acceptable even for the old SVX2 chip.

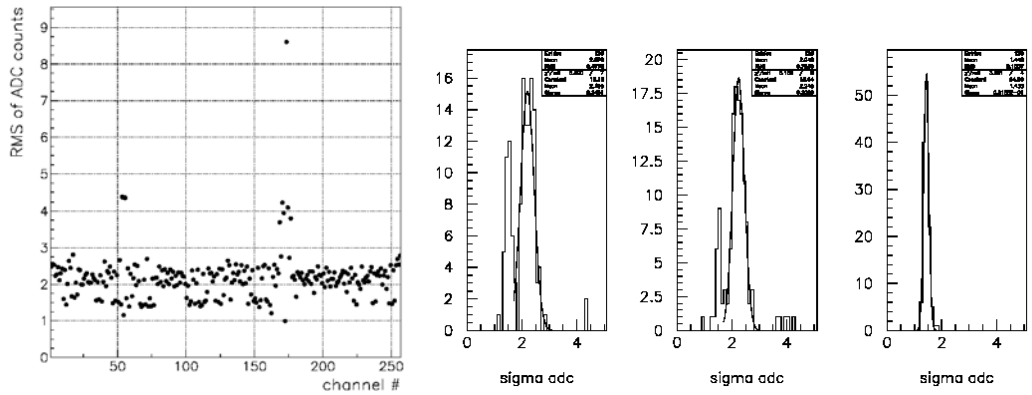

Figure 58 - The noise level for each channel (left). The channels with very high (or low) noise are caused by wire-bonding failure. The right plots show the projection of the left one for each of the three chips mounted on the hybrid. The first and second chips are used for the readout, while the third is a reference for the noise level.

The second study is a comparison of the noise levels with and without external shielding. Figure 59 shows the noise for each channel without the shielding. The noise level is increased by 1 to 13 ADC counts (corresponding to 1000 and 13,000 electrons, respectively), depending on the location. This noise increase implies the existence of RF pickup. Another interesting observation is the wing-like shape of the noise distribution. This is attributed to a shielding effect by traces themselves in the middle of cables, where neighboring traces work as a shield for each other; this effect is less significant at the edges of cables. This result unfortunately indicates that the analog cable indeed works as an antenna, and that shielding of the cable is crucial.

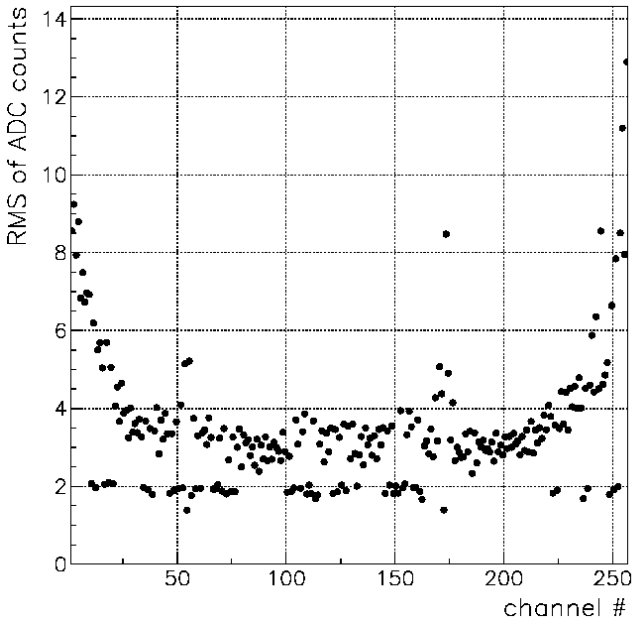

Figure 59 - The noise level for each channel. The Run IIb L0 prototype fixture is not shielded at all.

The next study is for the noise due to capacitive coupling of external sources to the analog cable. We placed a piece of aluminum foil under the analog cable. The aluminum foil was not grounded and thus was floating. Figure 60 shows the noise level for each channel, clearly indicating the capacitive coupling between the analog cable and the aluminum foil by two distinctive features. First, there is an even-odd effect. This comes from the difference in distance between the floating aluminum piece and the signal traces on the cable, *i.e.* one cable is laminated on top of the other and thus its distance is twice as great. Second, higher noise is observed near non-connected channels (those were bonding failures). The non-connected channels have signal traces without effective grounding through the preamplifier, leading to stronger capacitive coupling to the aluminum foil.

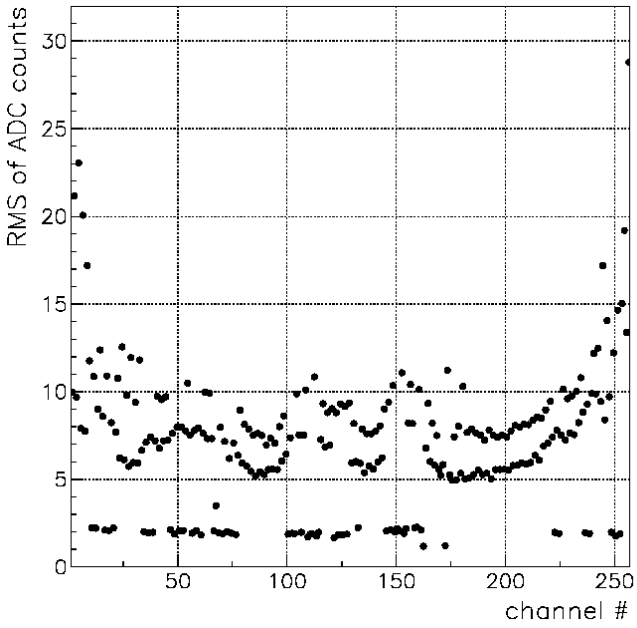

Figure 60 - The noise level for each channel. An aluminum piece without grounding connection is placed under the cable.

Figure 61 shows the pedestals and noise for a different prototype with a grounded shield. As one can see the grounding removes the noise and pedestal structure and reduces the noise to a level expected from the capacitive load.

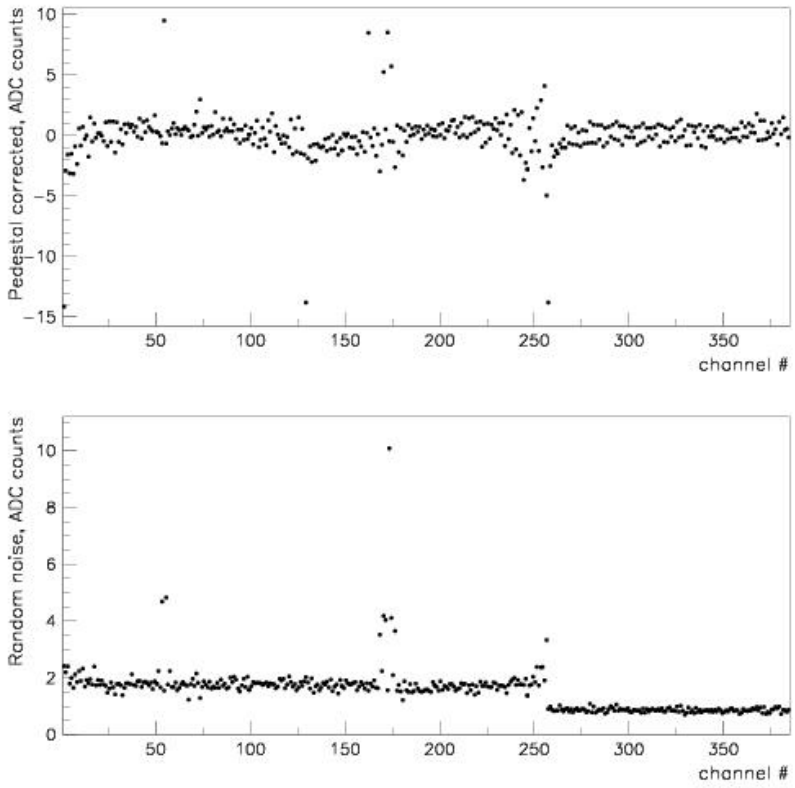

Figure 61 - Pedestal and noise for Run IIb L0 prototype with grounded shielding.

From the test results above, a particular concern for Layer 0 is the proximity of sensors to highly conductive K13C carbon fiber, which will be used for the mechanical support structures. These elements have the potential to produce strong capacitive coupling to the sensors, similar to what CDF experienced in Run IIa with L00 cooling tubes, and to what we have seen in the Run IIb L0 prototype. Therefore, it is imperative that all carbon fiber in the detector be effectively shorted to the bias filter grounds to prevent capacitive noise transmission to the sensor readout.

A test was conducted to determine the feasibility of shorting a prototype Run IIb L0 carbon fiber cylinder to a filter ground plane. The carbon fiber was driven with the source power from the network analyzer. A sensor/filter mockup constructed of aluminum and Kapton layers was mounted on the cylinder with the network analyzer input wired to the sensor aluminum layer, and both the source and input grounds wired to the filter plane. Transfer functions to the sensor were measured with different configurations for shorting the carbon fiber to the filter plane. Strips of 1 μm thick aluminized Mylar, 0.5 mil aluminum, or copper tape were attached across the filter and carbon fiber. The effectiveness of the grounding strips was tested with and without additional copper tape coupling to the carbon fiber. The aluminized Mylar strips were minimally effective in reducing power to the sensor. Aluminum and copper strips performed equally well. The power reduction was independent of the number of strips, but proportional to the amount of copper tape used to couple the strips to the carbon fiber, up to a maximum reduction of 40 dB at 1 MHz. Further studies determined that aluminum foil embedded in the carbon fiber provides

very good coupling for grounding to the filter plane. The embedded aluminum will have 2mm wide strip extensions that will be folded over and shorted to ground pads on the filter. Further details of the carbon fiber grounding studies can be found in section 5.10.

Based on the grounding scheme studied above, we plan to assemble another Run IIb L0 prototype that will be mounted on the carbon fiber structure, in which the carbon fiber is shorted to the bias filter ground through the 2 mm wide aluminum strip. Noise reduction by this proposed grounding scheme must be evaluated with a prototype module.

5.4 Hybrids

This section describes the hybrid design and related electrical issues. The circuits connecting the SVX chips to the low mass jumper cable are commonly called "hybrids." The hybrids will be based on the technology of thick film deposition on ceramics successfully prototyped for the DØ Run IIb detector and used in a number of high energy physics experiments including all CDF SVX detectors and the CLEO microvertex detector[26]. In our case, the 380 μm beryllia substrate will be used for Layer 0 hybrids because of its significantly better thermal conductivity than alumina.

Thick film deposition by screen-printing is a mature technology allowing for a minimal via size in dielectric of 200 μm and minimum trace width of 100 μm. Multi-layer designs are routinely achievable. Typical thickness of dielectric and metal layers are 40 and 7 μm, respectively. We have identified CPT, Oceanside CA and Amitron, NH as our potential vendors. Both companies have solid backgrounds in hybrid production.

The Layer 0 hybrid will have 2-chips. In addition to providing a secure mount for the SVX chips and cable connector, the hybrids also have capacitors for bypassing the analog and digital voltages and the detector bias. The low- mass flat cable connects to the hybrid with an AVX connector plug (hybrid side) and receptacle (cable side). These are 0.5 mm pitch, low profile 50-pin connectors. The CDF Run IIa SVX detector uses similar connectors with a low failure rate. Placement of the connector on the hybrid allows for easy testing of hybrids with and without attached silicon sensors during all phases of the hybrid and module production. This is essential for the modularity of the design and for quality checking during module production.

The SVX control signals and readout bus lines are routed from the connector to the SVX4 chips via 100 μm wide traces. The traces stop near the back edge of each chip, where they transition into gold-plated bond pads. Aluminum wire bonds connect these pads to the bond pads on the chips. The chip power will be routed from the connector on a power plane, and there will be a dedicated ground plane in the hybrid. The total number of metal layers is 6.

Figure 62 shows the top view of the Run IIb L0 hybrid prototype manufactured by Amitron in May 2003 (left side) and the hybrid part of the assembled L0 module with analog and digital cables (right side).

[26] Nucl.Inst.Meth. **A435**, 9-15, 1999.

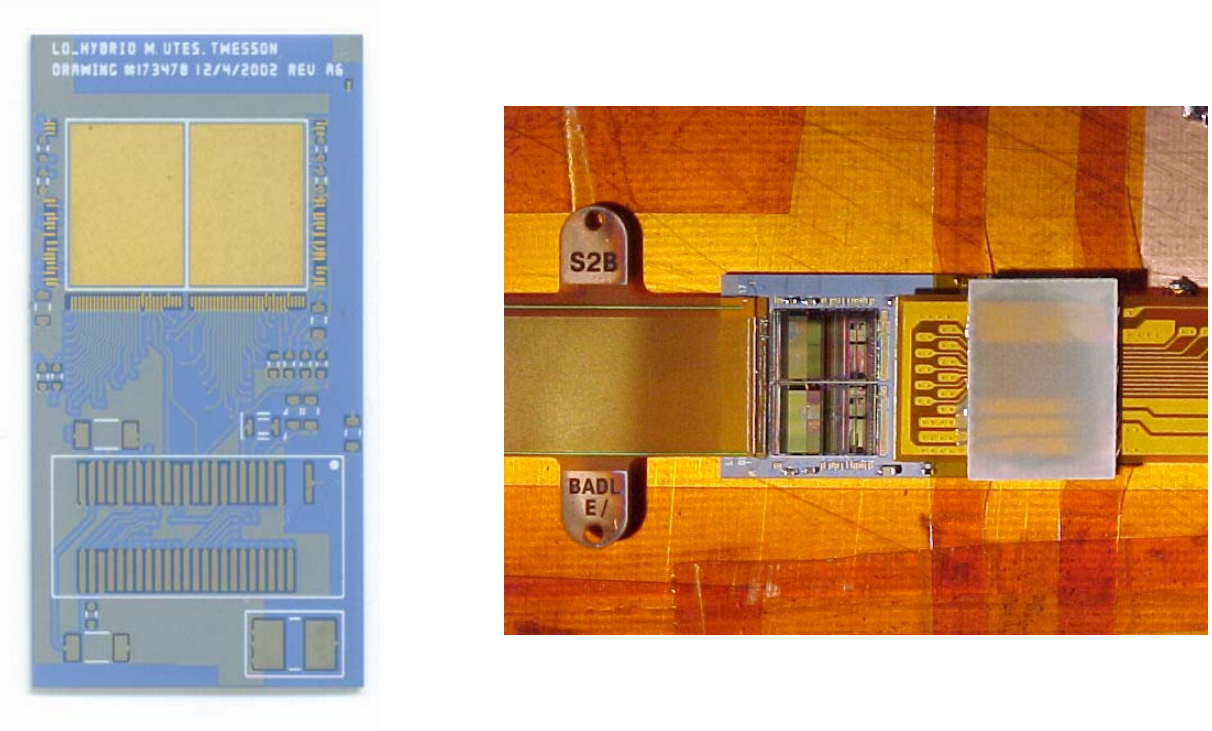

Figure 62 - Top view of a Run IIb L0 hybrid (left side) and hybrid part of the assembled L0 module with attached analog and digital cables (right side).

5.5 Cables, Adapter Card and Interface Board Overview

A primary goal of the Layer 0 readout chain design is to preserve as much of the Run IIa electronics and cable plant as possible. In particular, we want to keep: 1) the Interface Boards (IBs), located at the base of the central calorimeter, that relay digital signals between the sequencers and the SVX4 chip, supply both low-voltage power and high-voltage bias, and monitor current and temperature; 2) the high-mass cables, consisting of 3M 80 conductor cables and parallel coaxial clock cables that run from the IBs to Adapter Cards on the calorimeter face. Because of the complexity of these IBs, any required changes beyond the scope of component replacements or hand-wired jumpers will likely mandate complete replacement. Also, the space for connectors on the IB face is saturated. A required line count into the IB exceeding that available on the 80-conductor cables could not be accommodated.

As described below, the present design aims to preserve the IBs by replacing the Run IIa passive Adapter Cards on the calorimeter face with active ones that translate between single-ended (IB) and differential (SVX4) signals, and that also regulate supply voltages. The long (up to 2.7 m) Run IIa low-mass cables, which do not have differential-signal capability, will be replaced with new cables comprised of twisted pairs connected by small, passive Junction Cards to new, relatively short, low-mass Digital Jumper Cables.

5.5.1 Digital jumper cables

Digital Jumper Cables (DJCs) carry digital signals and power between the hybrids and the Junction Cards, where they connect to the Twisted-Pair Cables. In all, each DJC carries 11 pairs of differential signals, 6 single-ended signals, 5 sense lines, 2 power voltages and ground, and sensor bias. They are 14.7mm wide flex-circuit striplines similar to the low-mass cables used in Run IIa, which minimize the amount of material in the sensitive volume. Although shorter than the Run IIa cables, they are narrower and carry more signal traces, so that the feature size is 20% smaller. Run IIb L0 DJC's were expected to be approximately 45 to 65 cm long.

A DJC is needed for each hybrid in the detector. Signal traces 125 μm wide with 300 μm pitch, and also broad power and ground traces, are located on both sides of a Kapton dielectric 102 μm thick. A 50-pin, 0.5 mm pitch, 3.0 mm high AVX 5046 connector is soldered to pads at the Junction Card end, and the default design (pending further study of clearances) is to use a 2.5 mm high AVX 5087 connector at the hybrid end. The DJC's are reinforced by thin G10 backing behind the connectors to make them more robust during handling. Photographs of one end of a 50 cm prototype DJC (before connector installation) are shown in Figure 63 and Figure 64.

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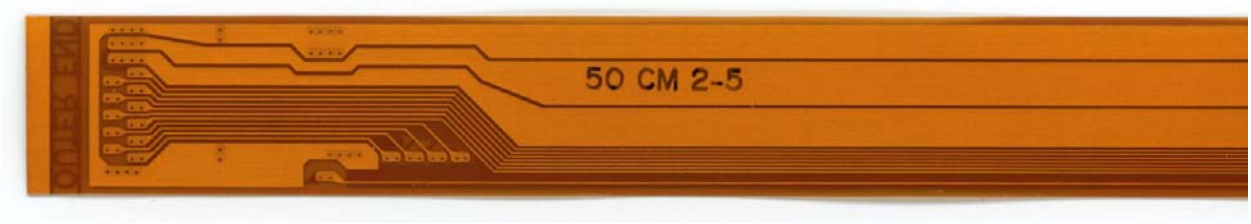

Figure 63 - Run IIb Digital jumper prototype cable: side opposite the connector.

Figure 64 - Run IIb Digital jumper prototype cable: connector side.

The prototyping program has qualified three vendors (Honeywell FM&T, Century Circuits, and Basic Electronics, Inc.) as well as validating the design. All three vendors have successfully produced both 50-cm prototypes and longer prototypes 86 to 100 cm long. Century has also made 300 50-cm DJC's of the same design for use in Run IIb silicon upgrade test stations.

Hybrids stuffed with up to 10 SVX4 chips have been successfully read out with a 50 cm DJC. In addition, the signals on prototype cables 50 cm and 100 cm long have been examined in detail. It was found that signal quality after 100 cm is good, measured impedances (107 ohms for

differential lines, 61 ohms for single-ended lines) are close to design values, and cross-talk is negligible for differential lines and acceptable (≤13%) for single-ended lines.

A setup for production testing of DJC's was established at Louisiana Tech, and most of the Run IIb prototype and test station cables have now been checked. The high-voltage trace gives no problems, even above the required 1000 V, and the yield of cables without shorts or opens has been good once the G10 backing was routinely included.

It is anticipated that the Digital Jumper Cables that will serve as an element of the proposed Layer 0 detector will be based upon the prototype developments made as part of the Run IIb silicon project.

5.5.2 Junction cards

Junction Cards are impedance-controlled passive boards that mate Digital Jumper Cables with the Twisted-Pair Cables that run to the Adapter Cards. They will be mounted near the present location of the Run IIa H-disks, and will have a maximum size of 30×100 mm^2. Junction Cards must be mechanically robust and securely mounted. All attached cabling is stress-relieved whenever possible. The Twisted-Pair Cables will plug into 44 pin Omnetics connectors, while the Digital Jumper Cables plug into 50-pin AVX 5046 connectors. Large 100 micro-farad capacitors are required for proper voltage regulation of SVX4 power.

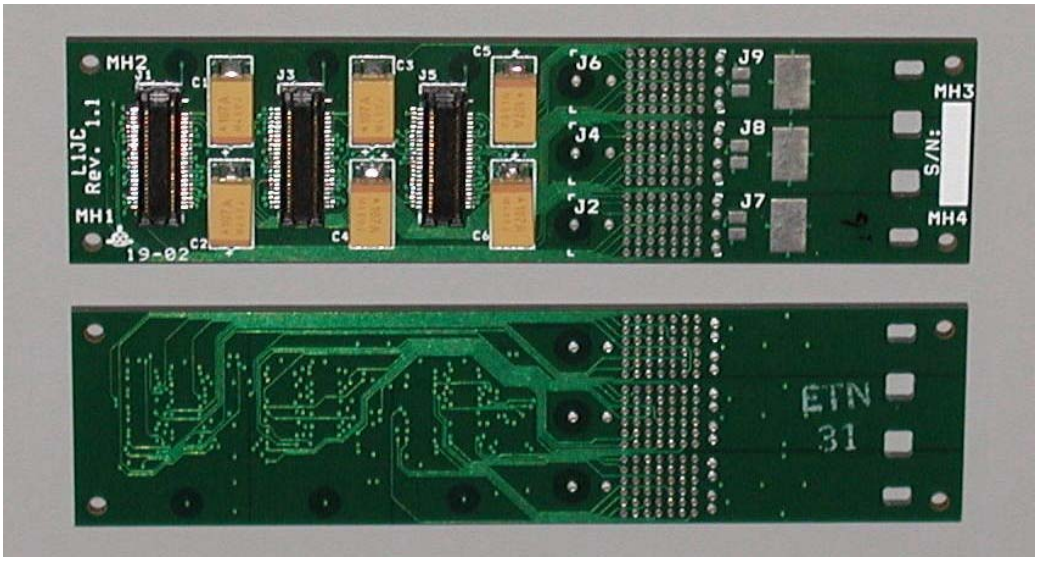

Figure 65 - Run IIb prototype three channel junction card (this version requires solder connection of signal lines).

As of September 2003, prototypes for three channel and two channel Junction Cards were in hand. Figure 65 is a photograph of a Run IIb prototype three channel Junction Card. This version requires that the lines in the twisted pair cable be soldered to pads on the junction card. Figure 66 is a photograph of one side of a two channel card which uses Omnetics connectors to make up the data line connections.

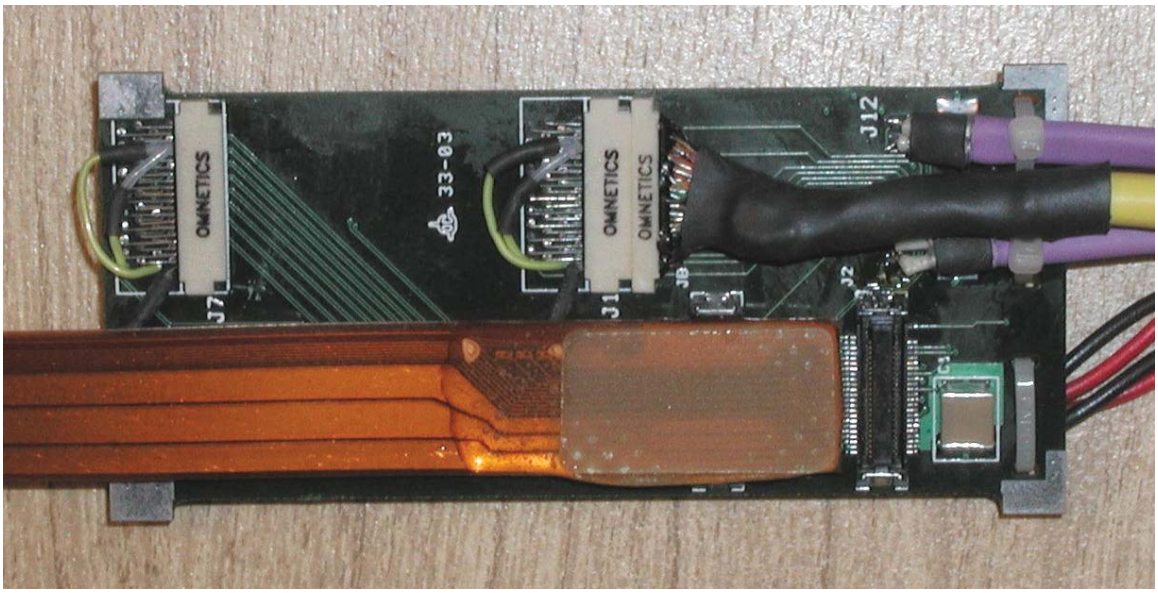

Figure 66 - Run IIb prototype two channel junction card. Twisted-pair cables plug into the light-colored Omnetics connectors on the top edge of the cards. The purple coax cables carry clock signals. Power lines are soldered on the other side of the card.

5.5.3 Twisted-pair cable

The Twisted-Pair Cable, approximately 2 meters long, connects the Junction Cards and Adapter Cards. As illustrated in Figure 66, the twisted pair cable is terminated with Omnetics connectors. The cable mass is not a major issue because the cable is outside of the tracking volume. The total outer diameter of a twisted-pair bundle can be as small as 5 to 6 mm.

The twisted pairs were chosen because 11 of the signals used by the SVX4 chip are differential. The 5 slower single ended lines will also use twisted pairs. The cable assembly has 2 power lines and their returns, 1 HV line and its return, 15 signal twisted pairs, one temperature sensor twisted pair and 2 voltage sensor pairs. The clock signals are transmitted via two coaxial cables in the same assembly.

Figure 67 specifies the connections between the Run IIb junction card and adapter card.

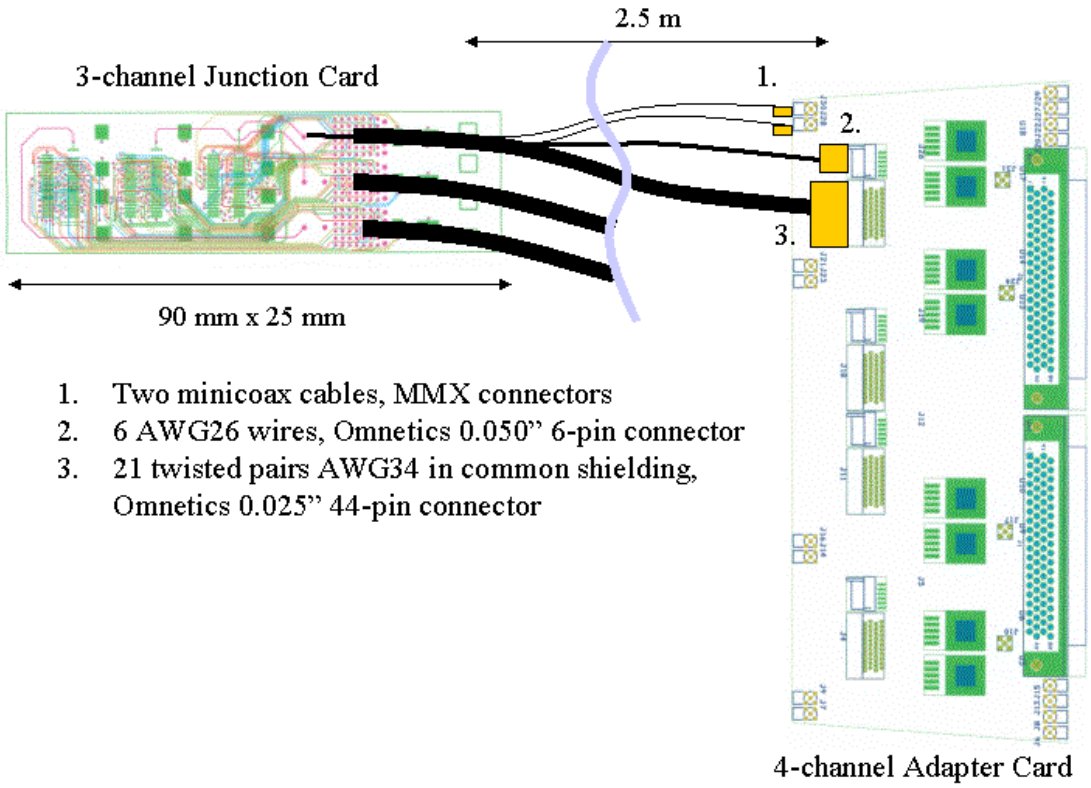

Figure 67 - Schematic connection between the Run IIb junction card and adapter card.

Figure 68 shows Run IIb prototype cables for the twisted pair cable assembly; from left to right: two connectors for micro-coax cables, 44-pin Omnetics connector for signal pairs, 6-pin Omnetics connector for HV and power lines. The signal twisted pair was produced by New England Wire and was terminated to the connector by Omnetics.

Figure 68 - Prototype cables for the twisted pair assembly; from left to right: two connectors for micro-coax cables, 44-pin Omnetics connector for signal pairs, 6-pin Omnetics connector for HV and power lines.

5.5.4 Adapter card

For Layer 0, new active Adapter Cards will replace some of the passive cards now mounted on large "horseshoes" on the north and south faces of the calorimeter. These new cards will replace those used by the H disks being removed from the detector. The adapter cards 1) translate single-ended TTL logic signals from the Interface Cards to differential signals to and from the SVX4 chips, 2) regulate the 2.5 volt SVX4 supply line to within the narrow 250 mV tolerances of the SVX4, and 3) generate an extra control signal needed by the SVX4 logic. To use the limited mounting space more efficiently, each Adapter Card will service two or four channels. Each pair of channels requires an 80-pin mini-D connector to interface with the High Mass Cables, and two fine-pitch AVX connectors on the Twisted-Pair side. Adapter card power and power for the SVX4 chips is supplied through the 80-conductor cable.

Fifteen Run IIb adapter card prototypes have been built and have been in use for some time to readout hybrids, modules, and full staves successfully. The heat output per channel (two hybrids) adapter cards is estimated to be 1.5 W if no changes are made to the current Run IIa low voltage system so the heat load transmitted via conduction to the mounting plate (horseshoe) is minimal and additional cooling of this plate may not be needed. This heat load drops about a factor of two if dedicated supplies are used.

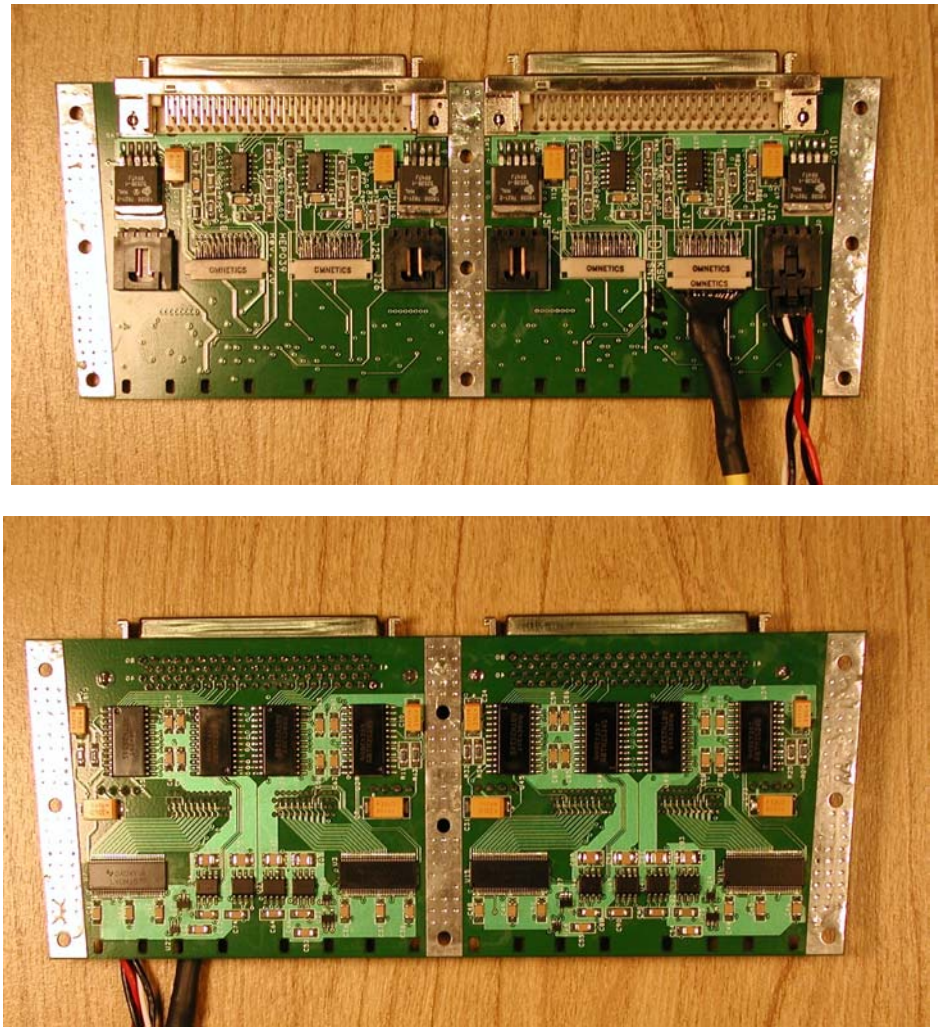

Figure 69 - Top and bottom sides of a Run IIb prototype revision 2 adapter card. This version handles four hybrids.

Additional engineering of the adapter cards may be required if it is determined that the Layer 0 detector ground must be isolated from the rest of the detector. In this case we would need to isolate the single-ended control lines going to the SVX4 chips, the SVX4 power lead, and the silicon sensor voltage bias. Isolation of the TTL control signals would likely be done using Burr-Brown isolated couplers, which capacitively couple in and out signals to avoid ohmic connections. This type of grounds isolation is common in medical instrumentation design.

5.5.4.1 Purple card

A variant of the Adapter Card, called the "Purple Card", has been built for test stands for testing and burn-in of hybrids and sensors. The Purple Cards combine the functions of the Adapter Cards and Twisted-Pair Cables, and some functions of the Interface Boards such as temperature and SVX4 current monitoring circuits, in these simplified test stands; they serve as an interface between the same Stand-Alone Sequencers used in the Run IIa test stands and Digital Jumper Cables. As of Fall 2003, 75 Purple Cards have been built, and installed in burn-in and other test stands. Figure 70 shows a prototype Purple Card.

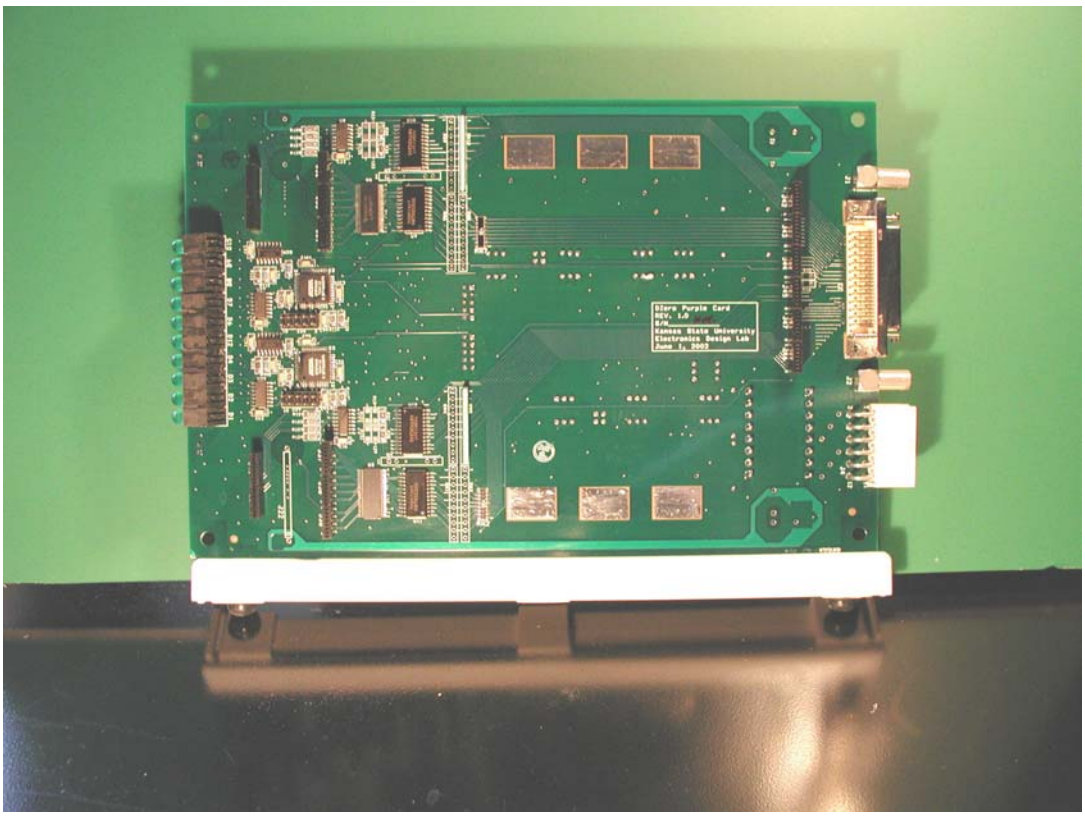

Figure 70 - View of a prototype Purple Card.

5.5.5 Interface board

In order to avoid the considerable expense of designing and building new Interface Boards (IB), the existing IBs must be recycled. All new features for Layer 0 are incorporated into the active Adapter Card. The IB detector bias distribution was tested to + 200 V, –100 V (including the switching relay) and should be safe for 300 V which is the expected maximum bias voltage expected after 8 fb^{-1}.

Required changes on the IB are minimal: reprogramming of 5 PLDs; and possible changes to priority-out signal threshold and hysteresis (this line was underdriven by the SVX2 chip). Experience on the teststands suggests that the 2nd change may not be needed.

5.6 Sequencer

The firmware in the sequencer needs to be adjusted for the difference between the SVX4 chip operating in the SVX2 mode and real SVX2 chip. The changes are rather straightforward and imply remapping of the SVX2 lines to SVX4 lines. The required remapping was shown in the section describing the SVX4 chip. Simultaneous operation of Sequencers reading out SVX2 and SVX4 chips will be verified in test stands.

5.7 Low Voltage Distribution

Currently VICOR switching power supplies [27] are used to provide power for the SVX2 chips and Interface Boards. For Layer 0 we intend to preserve those supplies and the distribution scheme through the Interface Boards.

The massive power lines from the VICOR supplies are split between different channels in the fuse panel. After the individual protection fuses, the power is distributed to the custom J1 backplane of 9U x 280 mm custom crates. The J2 and J3 backplanes of the crates provide connectors for the cable runs to the sequencers, while J1 contains connectors for low-voltage power for each Interface Board and up to eight dependent silicon hybrids, the 1553 connector and bus (used to monitor the SVX4 power and current, and hybrid temperature), and a connector to bring in 16 bias voltages and returns for eight hybrids.

5.8 High Voltage Distribution

Reliable high voltage operation is crucial to ensure the increased radiation tolerance of the new Layer 0 detector. Operation at voltages up to +300 V is specified for the Layer 0.

The high voltage bias will be applied to the backplane of the single-sided silicon sensors. For Layer 0 the bias voltage will be fed to a line on the analog cable and then will be connected to the backplane of the sensor near the end of the cable.

Despite the fact that Run IIa silicon detectors require operating bias voltages only within ±100 V, the specifications of the existing Run IIa HV power supplies should be adequate for the Layer 0 detector. Software compatibility and reliable operation of the current system are two other important considerations. Therefore, the most straightforward upgrade path for the HV system will be to keep the existing Run IIa system increasing the number of channels as needed.

In the Run IIa system, bias voltages are supplied from a BiRa VME 4877PS High Voltage Power Supply System[28]. It has been checked that the HV path through the Interface Board and 80-conductor cables can sustain up to 300 V and, therefore, can be preserved for bias distribution.

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[27] 4 kw MegaPAC AC-DC Switcher, Vicor Corporation, Andover, MA.
[28] Model VME 4877PS High Voltage Power Supply System Manual, March 1988, Bi Ra Systems, Albuquerque, NM.

5.9 Studies of the Expected Performance of the Run IIb Detector

Increased luminosity will result in high occupancy in the detector especially for the innermost layers. This has several implications for the readout performance. Two areas of concern, the SVX4 dynamic range and the detector readout time, were addressed in simulations that were performed as part of the Run IIb silicon detector upgrade project. Results of those studies provide some insights into the performance of the propose Layer 0 detector, and are therefore summarized in this Section.

The charge-sensitive preamplifier of the SVX4 chip integrates incoming signals and, therefore, needs to be reset regularly to prevent saturation. The saturated preamplifier will result in inefficiency of the detector. The reset time in SVX4 is equal to several hundred nanoseconds. Usually these resets are performed during the Tevatron abort gaps, which are periods of time within one revolution without collisions. Along with other modifications, the high luminosity regime of the Tevatron operation, may include reduction of the available abort gaps to possibly one per revolution. The current 36 bunches x 36 bunches operation allows for 3 abort gaps per revolution.

A full GEANT simulation with realistic clustering in the silicon has been used to estimate charge accumulated per strip after 450 minimum bias events. A scenario of 150 beam crossings before a reset with 3 minimum bias interactions per beam crossing was assumed. Figure 71 shows the charge per strip in the innermost layer after 450 minimum bias events. The left plot corresponds to the sensors in the central (closest to Z = 0) barrels. The right plot corresponds to the sensors in the end barrels. The central sensors are crossed by a larger number of particles while the incidence angles are shallower for the end sensors allowing for a larger deposited charge. As shown by arrows in both cases about 1% of strips will receive charge in excess of approximately 100 fC, which corresponds to 25 minimum ionizing particles. The dynamic range of the SVX4 chip was chosen to be 200 fC, leaving some margin for high luminosity operation. The expected inefficiency caused by the preamplifier saturation is expected to be less than 0.1%.

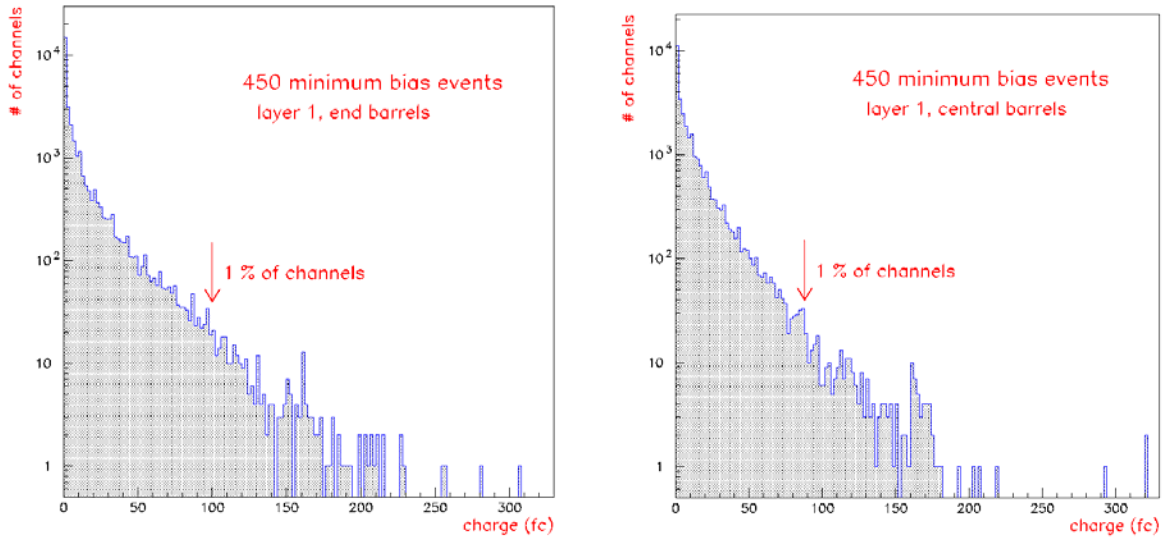


Figure 71 - Charge per strip in the innermost layer (labeled layer 1 in the figure) after 450 minimum bias events. The left plot corresponds to the sensors in the central, closest to Z = 0, barrels. The right plot corresponds to the sensors in the end barrels.

Another important performance issue for data acquisition is the readout time. A p-pbar interaction triggered for readout will be accompanied by several minimum bias interactions. To investigate a wider range of Level 1 triggers, several simulated samples were used: minimum bias, two jet and WH events. The maximum number of strips per readout cable in a layer was determined for each event. This number corresponds to the slowest chain of readout in this layer and is relevant to estimate the readout time for the detector and the associated dead time. The number of hit strips has been scaled by appropriate factors to account for the closest neighbors that normally are also included in the sparse mode readout. The factors were determined from the cluster size distributions and were typically around 1.7 for the cases without noise and 2.8 for the cases with noise. Figure 72 shows the maximum number of strips per readout cable as a function of radius for minimum bias events (left plot) and QCD two jet events (right plot). Each layer corresponds to two points in those plots from different sublayers. Four different cases were considered: without noise for the two thresholds of 4 and 5 ADC counts, and with noise (rms 2.1 ADC counts) for the same thresholds. The average simulated signal was equal to 20 ADC counts corresponding to a S/N ratio of 9.5. Figure 73 shows the maximum number of strips per readout cable as a function of radius for WH + 0 minimum bias events (left plot) and WH + six minimum bias events (right plot).

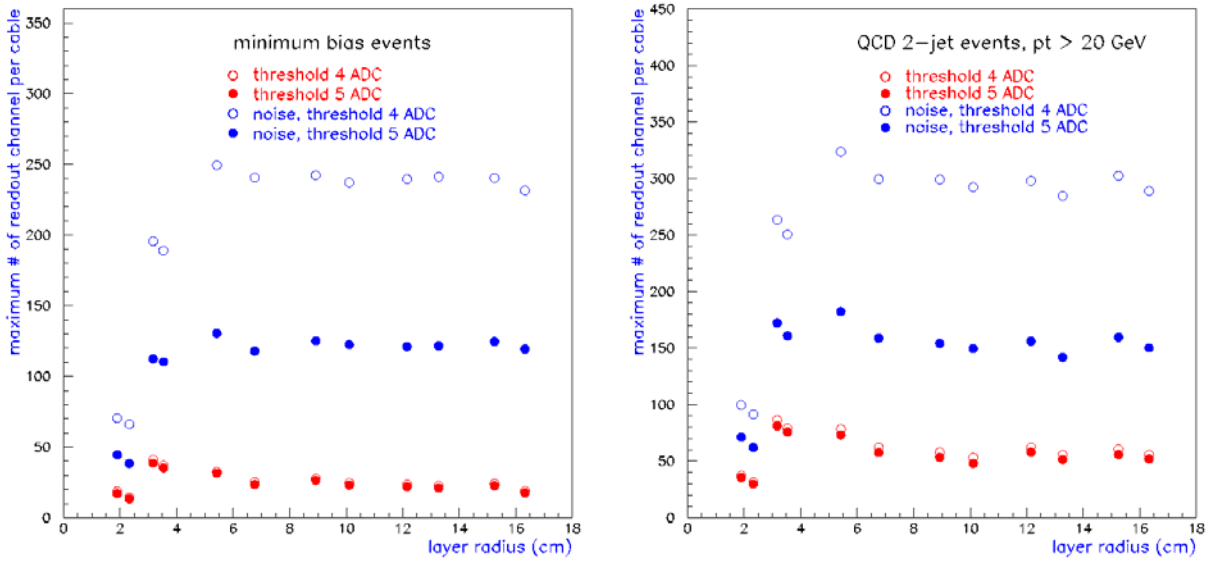


Figure 72 - Maximum number of strips per readout cable as function of radius for minimum bias events and QCD two jet events.

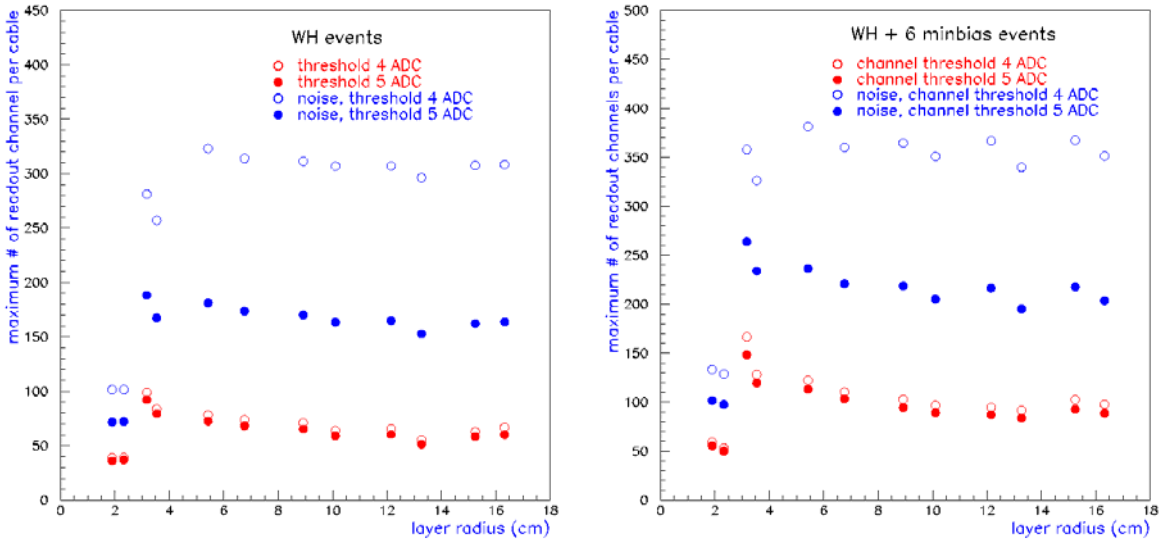


Figure 73 - Maximum number of strips per readout cable as function of radius for WH + 0 minimum bias events and WH + 6 minimum bias events.

5.10 Carbon Fiber Grounding Studies

A significant concern in the electronic and mechanical design of the detector is the proper grounding of carbon fiber elements. Highly conductive carbon fiber will be used for the mechanical support structures. These carbon fiber elements have the potential to exhibit strong capacitive coupling to the sensors. The CDF experience in Run IIa with L00 cooling tubes has shown that sensor coupling to nearby floating metal can be a very troublesome source of noise. It is imperative that all carbon fiber in the detector is effectively shorted to the bias filter grounds on the Layer 0 sensor high voltages cards to prevent capacitive noise transmission to the sensor readout.

The first test on the carbon fiber performed as part of the Run IIb studies was to verify its conductivity through capacitive coupling. Two identically sized plate capacitors were constructed: the first with one copper plate and one type K139 carbon fiber plate, the second with two copper plates. Both capacitors were measured to be 132±2 pF. Additionally, each capacitor was individually connected in series to a network analyzer to produce a high-pass filter. The transfer functions and break frequencies for the two capacitors were identical. Therefore, the conductivity of the K139 carbon fiber is high enough to make it virtually indistinguishable from copper in terms of capacitive noise transmission. Furthermore, K139 is the carbon fiber type that was to be used in the Run IIb L2 through L5 structures. K13C, which is more conductive than K139, will be used in the new Layer 0 support structure, where the proximity of sensors to carbon fiber is much greater.

Because the grounding concerns are most acute in Run IIb L0, a test was conducted to determine the feasibility of shorting a prototype L0 K13C carbon fiber cylinder to a hybrid or filter ground plane. The test configuration is shown in Figure 74. The interior of a castellated Run IIb L0 cylinder was driven with the source power from the network analyzer. A sensor/filter mockup constructed of aluminum and Kapton layers was mounted on the cylinder with the network analyzer input wired to the sensor aluminum layer, and both the source and input grounds wired to the filter plane. Transfer functions to the sensor were measured with different configurations for shorting the carbon fiber to the filter plane. One to four 1/8” wide strips of 1 μm thick aluminized Mylar, 0.5 mil aluminum, or copper tape were attached across the filter and carbon fiber. The effectiveness of the grounding strips was tested with and without additional cooper tape coupling to the carbon fiber. The aluminized Mylar strips were minimally effective in reducing power to the sensor. Aluminum and copper strips performed equally well. The power reduction was independent of the number of strips, but proportional to the amount of copper tape used to couple the strips to the carbon fiber, up to a maximum reduction of 40 dB at 1 MHz.

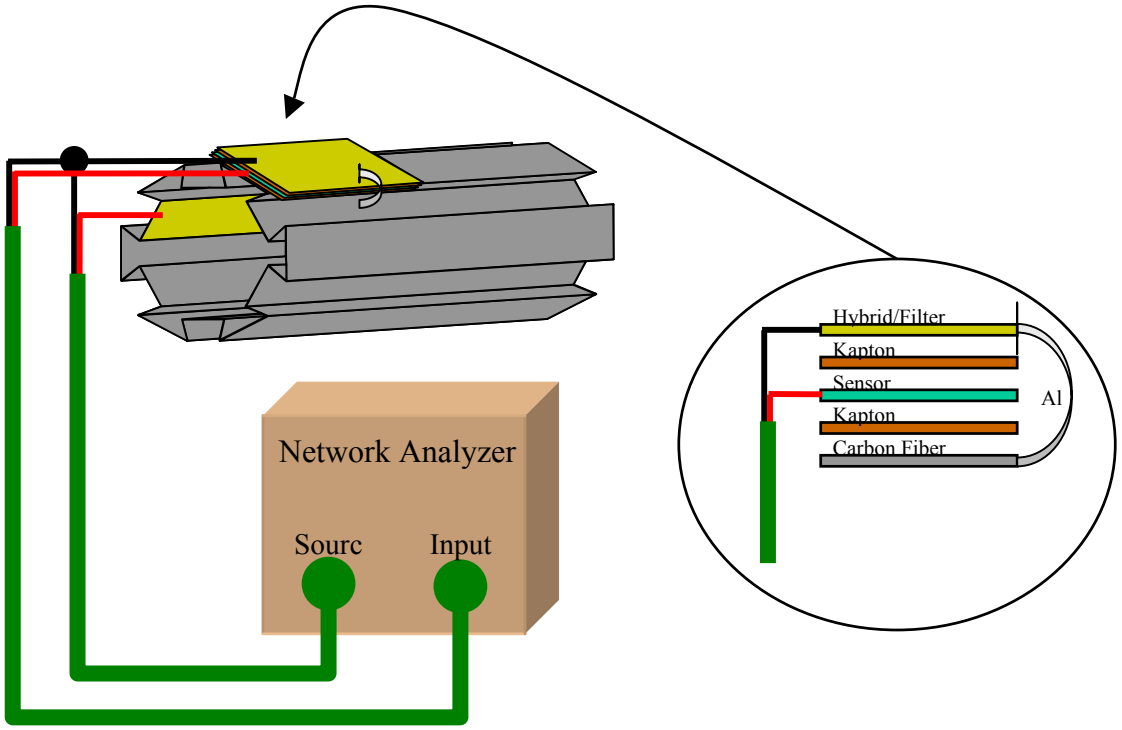


Figure 74 - Run IIb L0 grounding test setup.

A more systematic test of the relation of attenuation to the coupling area to carbon fiber was performed using a 36 in^2 parallel plate copper-carbon fiber capacitor. Figure 75 shows that increasing the area of copper tape coupling to the capacitor dramatically increased the attenuation up to a saturation point of about 4 in^2.

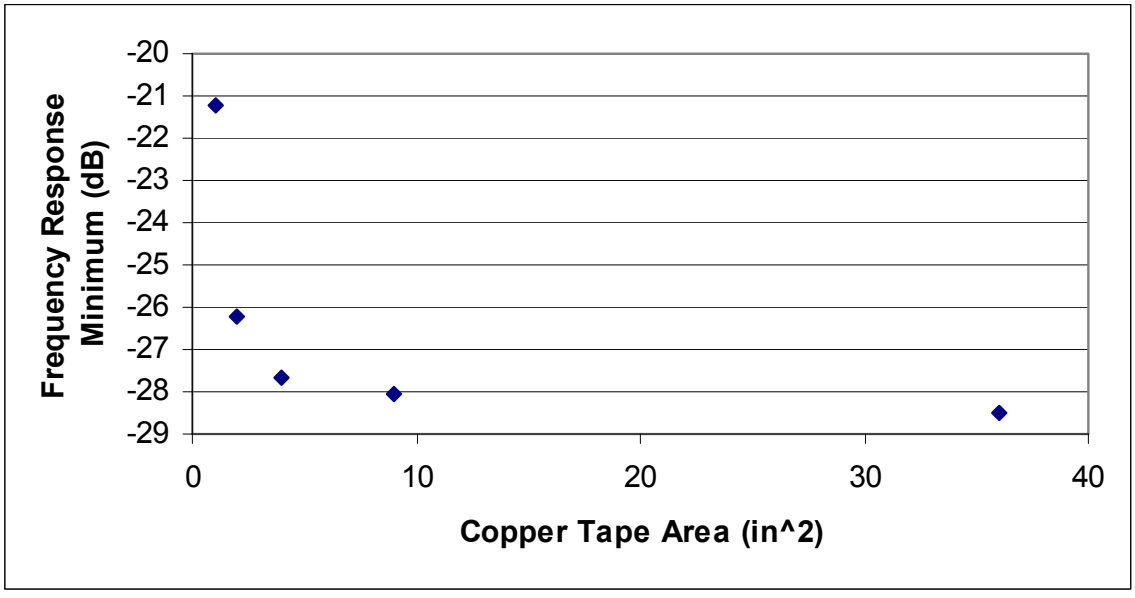


Figure 75 - Attenuation at 74 MHz as a function of coupling contact area.

Because copper tape coupling would be unfeasible in the detector, a coupling test was carried out using carbon fiber pieces with embedded aluminum foil and aluminized Mylar. A new sensor/hybrid mockup was built and mounted on different pieces of K13C carbon fiber with various amounts of surface area covered with embedded aluminum. The embedded aluminum extends out to grounding strips that fold over and attach to the hybrid/filter plane. A diagram of this setup is given in Figure 76. The coupling point on the actual planes will be 2 mm wide ground pads.

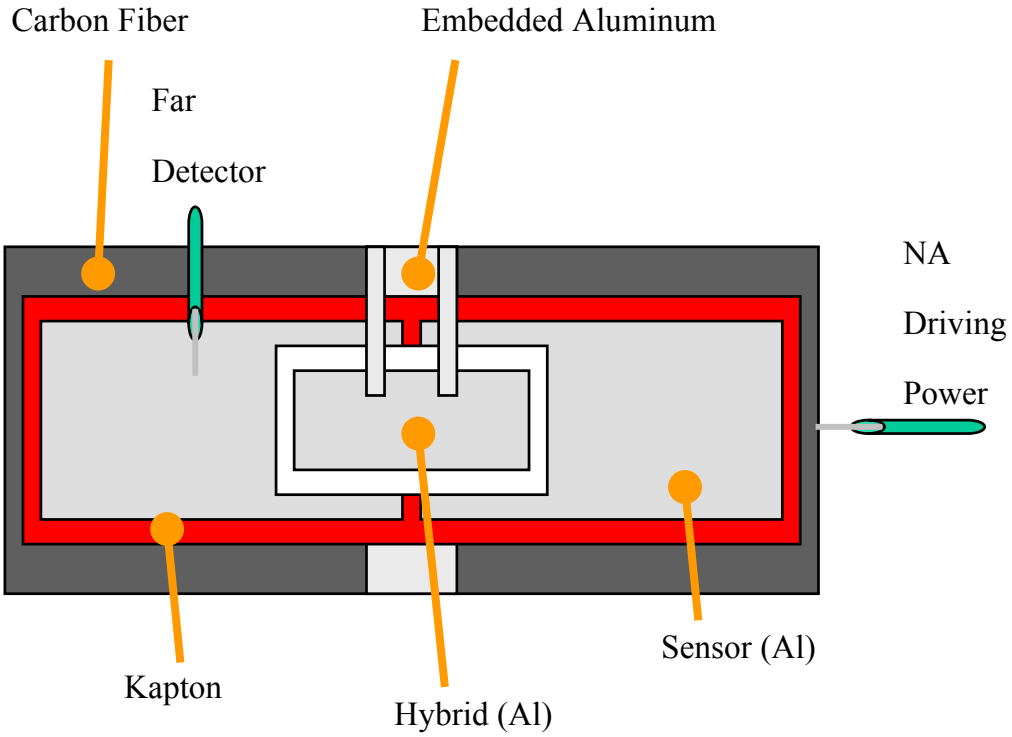


Figure 76 - Embedded aluminum coupling contact test setup.

Aluminized Mylar grounding produced significantly less attenuation than aluminum; about 10 dB less below 20 MHz. This test also verified that the attenuation is not affected by the size of the grounding strips. Measurements of transfer functions were taken with different areas of embedded aluminum and equal sized grounding strips. Those data confirmed that the attenuation increases with contact area to the carbon fiber. The maximum area of embedded aluminum tested was 4 in^2, giving a power decrease of at least 30 dB for all frequencies below 50 MHz. Coupling to carbon fiber through embedded aluminum was thus been shown to be an effective grounding technique.

The design adopted for grounding the Run IIb prototype inner layer structures was to co-bond Kapton flex circuits to the surface of the carbon fiber support structure (as opposed than imbedding aluminum). These flex circuits feature an exposed grid of 5 μm thick copper. Prototypes of pieces of these structures have been fabricated and successfully tested.

6 PRODUCTION AND TESTING

6.1 Overview

This section describes the full chain of testing of the individual components needed to build silicon readout modules and the assembly of modules into the Layer 0 detector. The essential building blocks of a detector module are the silicon sensors, the analog cable, the SVX4 readout chips, and the readout hybrids. Each component is tested as described below before it is assembled into a module. After assembly, the modules are tested again before they are mounted on the support structure. Testing of the full readout system is also discussed below.

The basic production and testing sequence is the following:

1. SVX4 chips are tested as described in Section 5.2
2. Bare hybrids are tested for continuity and shorts by the manufacturer
3. Bare hybrids are re-tested at remote institutions
4. SVX4 chips and passive components are surface mounted on the hybrids
5. Fully assembled hybrids undergo an initial functionality test
6. Hybrids that pass the functionality test are burned-in
7. Sensors are produced and tested at the manufacturer
8. Sensors are re-tested at Fermilab or remote institutions
9. Sensors and burned-in hybrids are assembled into a detector module.
10. Detector modules undergo initial functionality test at Fermilab
11. Detector modules that pass the functionality test are burned-in at Fermilab
12. Burned-in detector modules are subject to more detailed QA tests
13. Fully tested modules are mounted on support structure
14. Up to 6 detector modules are read out simultaneously

Aspects of the testing procedure are described in detail below.

6.2 Silicon Sensor Testing

Silicon sensors will be tested by the manufacturer and by DØ as described below. Sensor testing by DØ will take place either at Fermilab, or at one of the various testing centers that had been setup for the Run IIb silicon project. All electrical tests will be carried out in a temperature and humidity controlled environment, with the sensors placed in a light tight dark box.

We expect the manufacturer to perform the following tests:

1) Tests on each sensor

   a) Leakage current as a function of reverse bias up to 800 V at room temperature (T = 21 ± 1°C) and relative humidity (RH) < 50%

   b) Optical inspection for defects, opens, shorts and mask alignment (better than 2.5 μm)

   c) Depletion voltage measurement either by measurement of the capacitance between back-plane and the bias ring at 1 kHz frequency as a function of reverse bias, or by similar measurement performed on a test diode produced on the corresponding wafer.

2) Tests on each strip

   a) Capacitance value measurement and pinhole determination

   b) Leakage current at Full Depletion Voltage (FDV) and Room Temperature (RT)

   c) The total number of defective channels must not exceed 1%. Defectice channels are defined as:

      i) Pinholes – current through capacitor >10 nA at 80 V and RT

      ii) Short – coupling capacitor >1.2 times the typical value

      iii) Open – coupling capacitor <0.8 times the typical value

      iv) Leakage current above 10 nA/strip at FDV and RT

      v) Strips with bias and interstrip resistance values out of our specifications

3) Tests on test structure

   a) Poly-resistor value

   b) Sheet and implant resistivity

   c) Coupling capacitor breakdown voltage

The corresponding quality control data of the tests performed by the supplier will be provided together with each sensor on paper or in a computer readable format agreed upon by both parties. The QA program for silicon sensors will be performed at Fermilab or at remote sensor testing centers. We anticipate that tests a) through e) will be performed on all sensors, while the remainder of the tests will be performed on only a subsample or on test structures.

1) Electrical Tests

   a) Initial registration of the sensor in the database

   b) Visual inspection

c) I-V measurement

d) C-V measurement

e) Leakage current stability I(t)

f) Full Strip Test (AC scan)

g) Strip leakage current test (DC scan)

h) Polysilicon resistor measurements

i) Strip and interstrip capacitance

j) Metal series resistance

k) Implant sheet resistance

l) Flat band voltage measurements on MOS test structure (if available)

m) Interstrip resistance

n) Coupling capacitor and coupling capacitor breakdown value on test structure

2) Mechanical tests

a) Sensor thickness

b) Sensor warp

c) Sensor cut dimensions and cutting accuracy

Only sensors that meet all the qualification criteria will be used to build modules.

6.3 Hybrid Assembly and Initial Tests

Only one type of hybrids (2 chip-wide) will be used for this Layer 0 detector. The hybrids consist of several elements, which are assembled to form the final readout unit. The beryllia ceramic substrate contains a multi-layer thick film printed circuit. Passive components are mounted on the hybrid, as well as the custom SVX4 readout chip. An AVX connector allows a jumper cable to be attached to the hybrid to carry the digital signals to the downstream data acquisition system. Approximately 100 production hybrids will need to be assembled and tested.

The hybrid is to be constructed of alternating thick film layers of gold and dielectric built up onto a beryllia substrate. There are six conductor layers and five dielectric layers on the top side of the substrate. Some of the gold pads on the top layer must be aluminum-wedge bondable while others must accept solder or silver epoxy. Layers of dielectric may be added to the back side of the substrate in order to keep the finished hybrid flat to within 0.05 mm. Total thickness of the

finished hybrid must not exceed 0.8 mm. Thickness of the metal trace layers is specified to be 7 to 9 μm; ground and power plane layer thickness is to be 4 to 6 μm. The thickness of the dielectric layer is in the range of 40 to 60 μm, with a specified dielectric strength of 650V/mil or better. Laser cutting of the final outline should be accurate to ±2 mils.

During production of the hybrids, the vendor will test for continuity and shorts. The hybrids will undergo further testing and cataloging after receipt from the vendor. Each substrate will receive a unique identification number and its characteristics entered into a database. The testing starts with a visual inspection. Hybrids will be examined for visual defects and their mechanical tolerances will be checked. A full dimensional inspection will be performed on the hybrids using a coordinate measuring machine to verify that the substrates meet the required tolerances. The flatness of every bare hybrid will be checked as this is critical for clearances as well as for the thermal performance of the completed modules.

Test stands to check the electrical properties of the bare hybrids will exist at two university locations as well as Fermilab. These test stands will be used to check for continuity and shorts between each of the pads on the substrate and each connector pad. This test stand uses a Rucker & Kolls semi-automated wafer probe station, controlled through GPIB interface with a PC running LabView. Given a coordinate map of the hybrid circuit, the probe station stage positions each pad under a probe tip, connection is made through a GPIB multiplexing box, and a GPIB controlled multimeter checks for continuity or shorts between the appropriate connector point and the probe.

This testing procedure was tuned for use for the hybrids in the Run IIa SMT detector, and has been exercised on the Run IIb prototyp hybrids. We expect to probe every ceramic hybrid before they are sent for stuffing and wirebonding.

6.4 Test Stand Hardware

Essentially the same type of test stands will be used for all the electrical tests performed on the readout hybrids and the detector modules. These test stands are based on the Stand Alone Sequencer Board (SASeq), which was developed at Fermilab and successfully used in Run IIa. The two-channel SASeq board is a self-contained data acquisition card designed to interface to the SVX chips. Its basic function is to control the SVX chip for data acquisition, collect the SVX data when a data cycle is requested, and to relay the data to the processor in the crate. We plan to utilize the test stands already completed and commissioned for the Run IIb silicon project, currently located at SiDet and at various remote institutions. 4 different types of fully functional SASeq based test stations are available for the Layer 0 project

1. hybrid burn-in station for burn-in of hybrids

2. module burn-in station for burn-in of detector modules

3. 1-Saseq station for fast functionality test and debugging of modules and QA tests, with stations at Fermilab and at remote institutions

4. 3-Saseq station (6 channels each) for simultaneous read out of up to 6 modules during mounting in the final support structure

A Module burn-in station consists of two Cooling Racks and a VME Rack between them. A Hybrid burn-in station consists of a Shelve Rack and a VME Rack. Module burn-in stations can be used for hybrid burn-in. The base hardware unit for the burn-in stations is shown in Figure 77. The Burn-in Crate configuration for module burn-in is shown in Figure 78. It consists of a VME crate that contains a Bit-3 VME controller card, sixteen SASeqs, a scanning 12-bit 64 channel analog-to-digital converter board (VMIVME-3113A) for temperature measurement, and a master vertical interconnect board for high voltage crate control. High voltage supply sources are located in a separate VME crate.

The HV VME crate for the burn-in stations contains four VME 4877PS Motherboards and a slave vertical interconnect board for high voltage crate control. Every Motherboard carries eight HV pods. Thus, the HV crate provides 32 independent voltages for silicon detector biasing and supports monitoring of the detector currents. The 4877PS Motherboard allows the voltage to be set from 0 to 5000 V, with a maximum current of 2mA per channel. To ensure the safe operation of the burn-in stations, the over-voltage hardware protection of the HV supply will be set to 300V.

The interface between the hybrids and the SASeq is provided in Run IIb by a circuit board dubbed the Purple Card. It is the functional analog of the Interface Card and Connector Adapter Module used in Run IIa. The Purple Card is located close to the device under test inside the Cooling Rack. Every Purple Card has two independent channels and is used as a bi-directional interconnect between the SASeq and the Hybrid through the Digital Jumper Cable (DJC). The board contains the logic to control the power of the SVX chip as well as the HV. The board also prepares the data for the temperature measurement. All low voltages are fused on the Purple Card. The Card is equipped with test points and LED's to monitor the functionality and provide diagnostic capabilities if they require servicing.

Each SASeq is connected to a Purple Card by a 10 foot long 50-conductor cable with impedance of 82 Ohms. Three low voltage power supplies are used to supply the two operating voltages (AVDD, DVDD) needed by the SVX chips and to supply the voltage to power the Purple Card. Low Voltage Distribution wire buses are located on the side of each Cooling Rack or Shelve Rack and are used for the distribution of the SVX power and the Purple Card power for each of the sixteen Cards.

The Hybrid burn-in station and the Module burn-in station only differ in two aspects, which are the High Voltage crate and the cooling system. The Module burn-in stations need a separate VME crate to house the high voltage modules to bias the detectors, which is not needed for the Hybrid burn-in stations. For the one-SASeq and three-SASeq test stations the HV module is located in the same VME crate as the SASeq. The second aspect in which they differ is the cooling. The Module burn-in stations are outfitted with a cooling system to operate the detectors at low temperature. Up to 16 detectors are placed on 8 shelves inside a Cooling Rack that is thermally isolated. The chiller temperature is set to 5C, and the detectors will run at temperatures between 10C and 15C, depending on the number of chips on the HDI and on the water flow rate. Each detector module is placed on a custom made, 17 x 3.5 inch aluminum Cooling Plate (see

Figure 79), designed to accept any kind of Module. Every Cooling Plate is equipped with a pipe for cooling water and special holes to provide nitrogen flow through the storage box that encloses the device under test. Two Cooling Plates together with the Purple Card and signal cables are placed on plywood board. This board, called the Slider Plate, is equipped with sliders to simplify loading and unloading of the devices under test (see Figure 80). Plywood is chosen because it is a cheap, thermally non-conductive material that helps minimize possible risk of condensation on surfaces inside the Cooling Rack. Every Slider Plate has its own water and nitrogen pipe.

A control panel attached to the rack side provides control of the water and gas flow. One chiller supplies two control panels. A software based interlock system monitors the temperature on each device and shuts off the power in the event the temperature exceeds 50C, to avoid melting of the epoxy used in detector assembly.

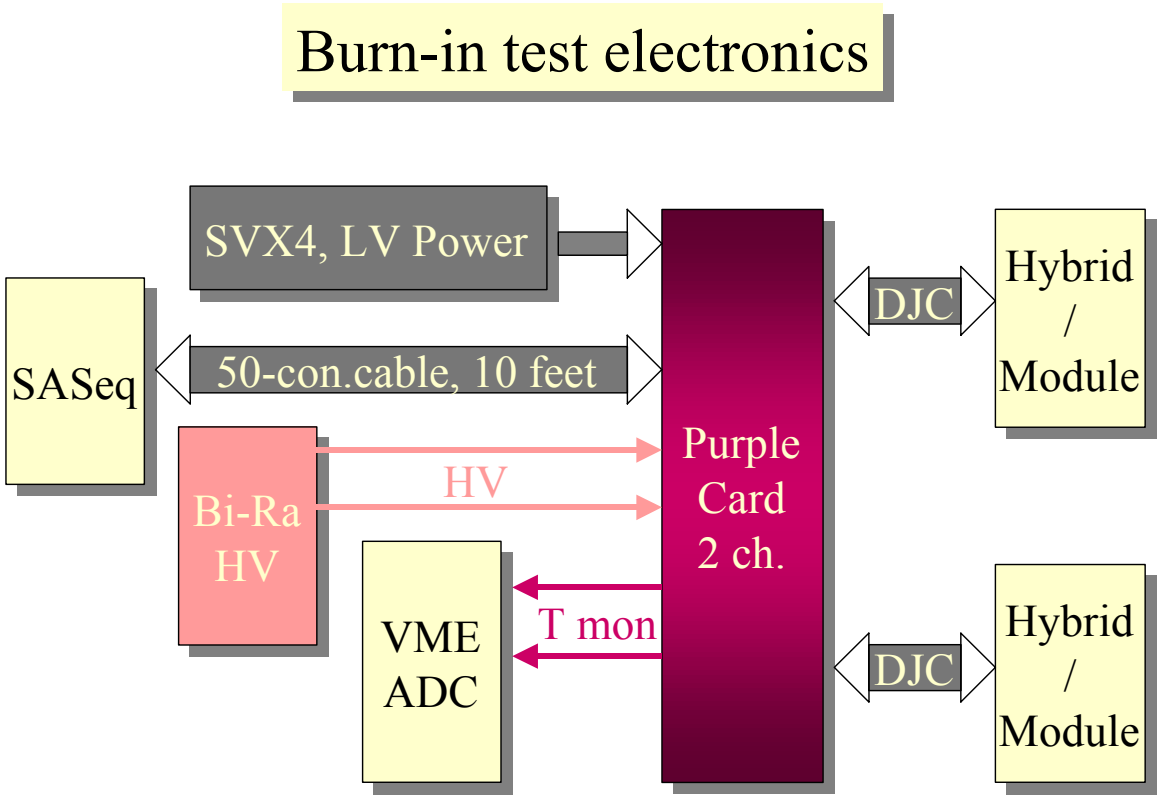


Figure 77 - Base Unit of Burn-In Test Electronics.

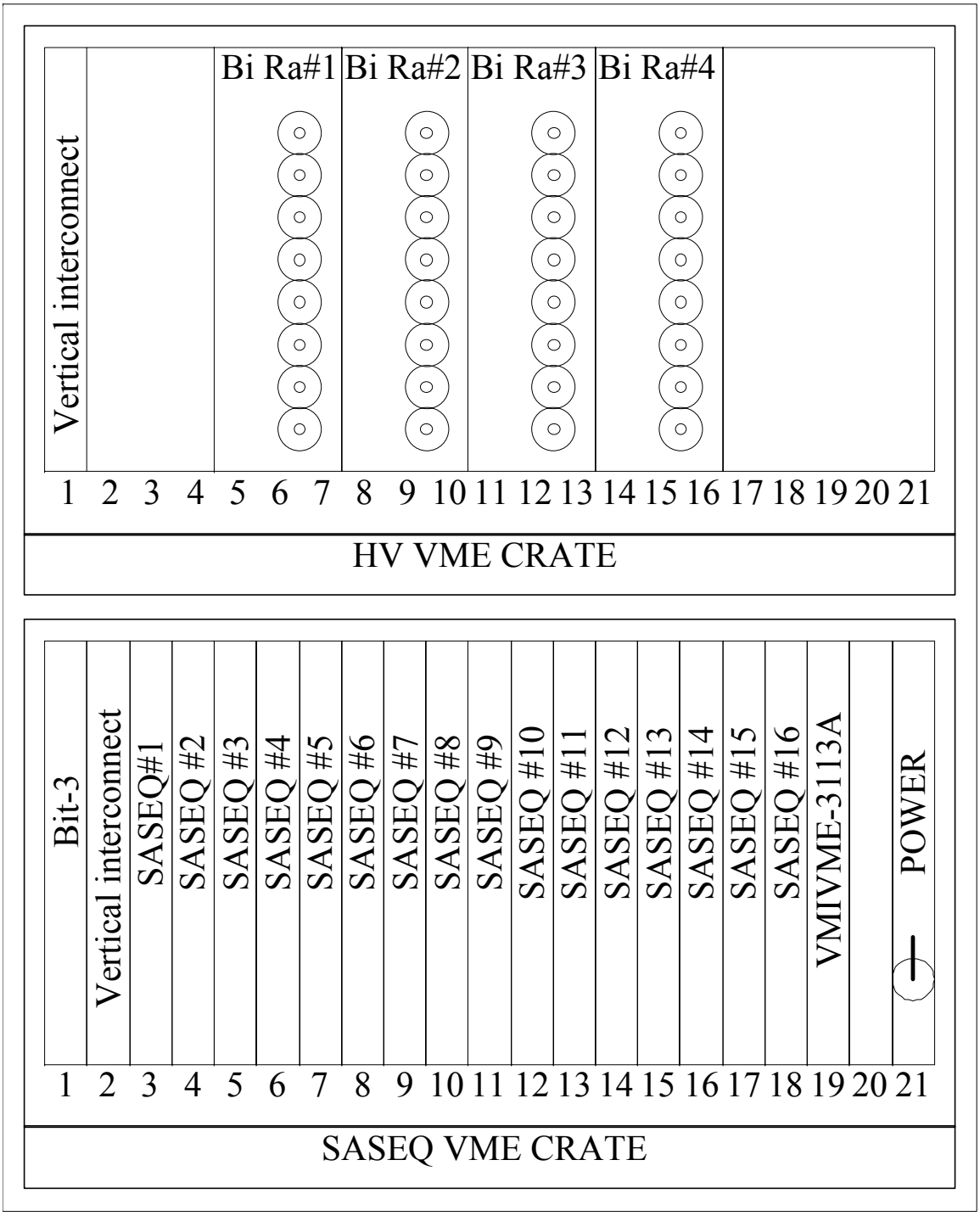
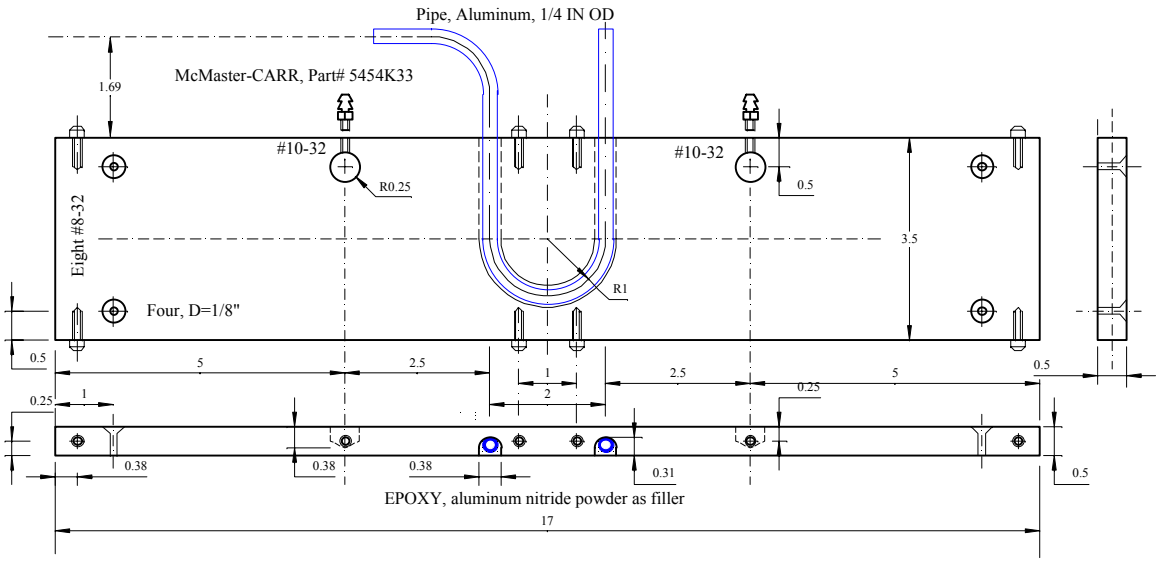


Figure 78 - Burn-in Test Crates.



BURN-IN TEST Cooling Plate.
ALUMINUM, 17 x 3.5 x 0.5 INCH

Figure 79 - Cooling Plate.

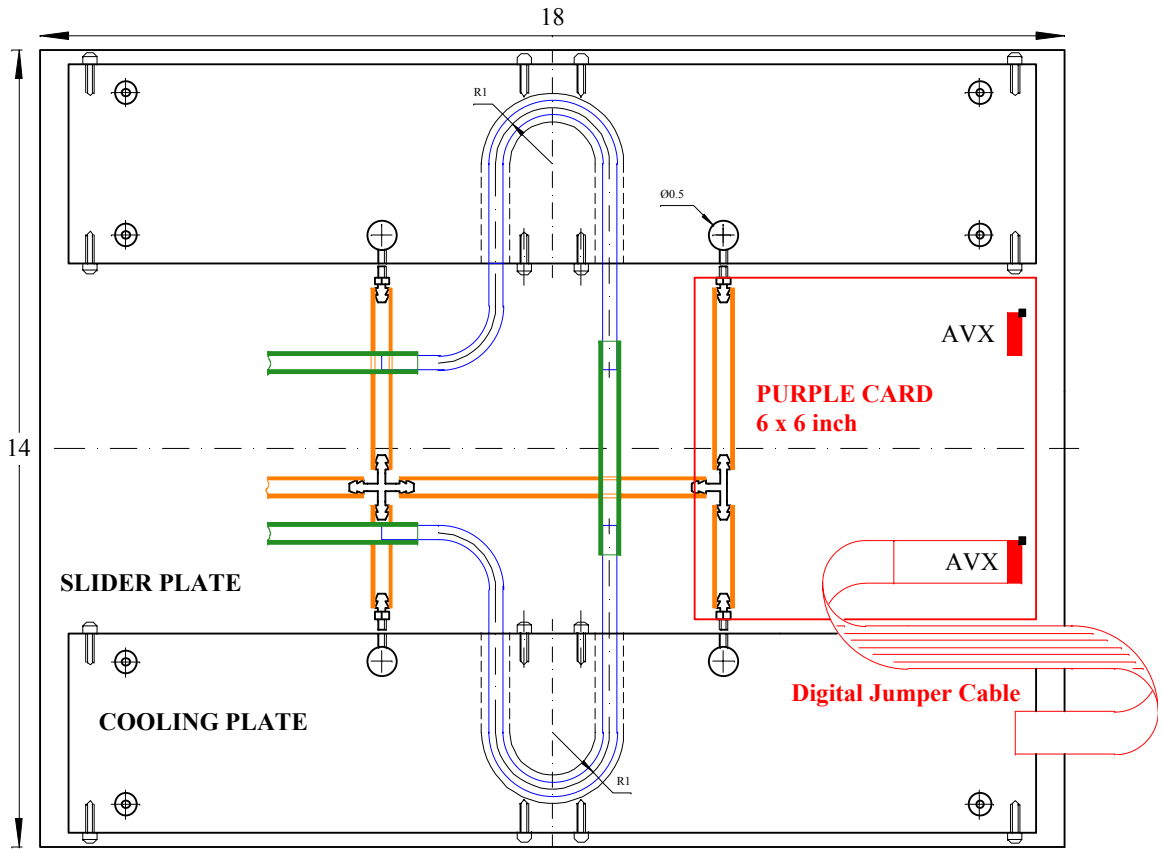


Figure 80 - Slider Plate.

6.5 Fast Functionality Test for Stuffed Hybrids

Once the bare hybrid is ready for surface mount of components, it will be shipped to the stuffing vendor. The vendor will surface mount the passive components, including the AVX connector, using a pick and place machine, perform a simple continuity and short test, attach the SVX4 die to the beryllia substrate using silver epoxy, and then wirebond the SVX4 chip to the substrate. The vendor will ship the finished hybrids back to university collaborators for functional testing.

The initial functionality test at the collaborating universities includes a visual inspection (to ensure that the components were mounted correctly and wire bonds were made to the right pads), and examination of distributions of pedestal and noise as a function of channel number for each of the SVX4 chips on the hybrid. The behavior of the hybrid will also be tested using a large number of successive downloads and in cal-inject mode. The visual inspection is done using a high powered microscope. The purpose is to obtain quick feedback for the stuffing vendors, including general wirebonding problems (too-long tails for example) and to attempt to ameliorate any problems before electrical tests. Typical “repairs" at this point may include manually straightening out bent bonds, identify missing or broken wire bonds for repair in-house, locating SVX4 chips with obvious defects, and also to blow off or pick off debris from previous handling. A K&S manual wire bonder is available at each university hybrid testing site for these quick repairs.

After the visual inspection, there will be a static electrical test to check for power shorts and to verify the connection of the platinum temperature measuring resistor. Hybrids with shorts will be set aside for possible debugging. The functional electronic readout tests are performed using 1-SASeq stands at each university. These stands are already in place from the Run IIa detector and have been modified for use with the SVX4 chip. This is the basic test of download and readout. We require 100 successful downloads, and error free readout of 10,000 calibration and pedestal events.

Download failures are, if possible, localized to a single chip using a manual probe station in conjunction with an oscilloscope and logic analyzer, and defective SVX4 chips marked for replacement. Hybrids with problems are scanned at high magnification (50-250X) to search for chip and other defects. For the Run IIa hybrids, in about 50% of the download and readout failures cases, an SVX2 chip flaw was visible. For Run IIa the repair statistics were:

- Diagnostic success was stated to be >70%, meaning that at least 70% of the download and readout failures, when localizable to a single chip, could be recovered.

- About 30% of the hybrids with shorts were recovered, in some cases by burning off debris at “high" current (less than 1A in order not to melt wire bonds), or by manipulation of hybrid tails.

The initial yield of working hybrids that were stuffed for Run IIa was 70% and varied significantly between different hybrid types and batches. The yield after repairs for working stuffed hybrids was around 90%.

The plans for testing are being prepared assuming yields such as those found in Run IIa for the stuffing and wirebonding vendors, which we believe to be conservative. University collaborators will interact with vendors, and perform the initial functionality test and needed repair. Hybrids that pass the functionality test are then put through burn-in tests at Fermilab. Hybrids that pass the burn-in test are used to assemble detector modules.

6.6 Module Assembly

Information about the depletion voltage and the number of bad strips will be provided as input to the testing and assembly group and taken into account when choosing sensors for a particular detector module. Only those hybrids meeting the desired criteria will be matched to silicon sensors and assembled into detector modules.

The module assembly process consists of three distinct operations. The first operation is the preparation of the sensor. This involves lamination of a Kapton foil to the backside of the sensor, primarily for electrical insulation of the high voltage from the adjacent support structure at ground potential and installation of the HV filter card on the sensor. The Kapton foil includes a small metallized trace facing the bottom of the sensor to bring the high voltage from the HV filter card to the back plane as well as a trace on the opposite side to bring ground from the HV filter to the carbon fiber support structure. The Kapton foil is installed first, then the assembly is flipped over and the HV filter card is mounted on the top of the sensor. Finally the tabs of the Kapton circuit are wrapped around the edge of the sensor and connected to pads on the HV filter card using silver epoxy for the electrical connection and structural adhesive to secure them in place. Prototype foils were prepared for L0 and L1 of the initial Run IIb detector and successfully laminated on sensors and modules.

The second operation is the preparation of an analog cable pair. This involves lamination of each analog cable to a ceramic spacer at the two ends in the bond pad region. These spacers supply the required rigidity for bonding the cables to the sensors and hybrids. After each cable is prepared, the two cables are laminated together by bonding the ceramic spacer of the upper cable directly to the top surface of the lower cable. Tooling has been designed and prototyped which provides adequate alignment of the two cables using laser-drilled holes in ears of the cables engaged on dowel pins. The same tooling provides for vacuum hold-down of the ceramic spacers and alignment of the spacers to the cables with dowel pins.

The third operation involves attachment of the analog cable pair to the sensor and hybrid. Again, the analog cable pair engages pins on tooling which aligns the sensor and hybrid using alignment dowels and vacuum hold down to locate the sensor and hybrid. Final electrical connections between the sensor, HV filter card, analog cables and hybrid are then made using wire bonding.

There are 48 modules to be installed. We anticipate making approximately 50% spare assemblies, so a total of perhaps 72 modules. Given this small number of units to build, we anticipate spending two or three months assembling modules at a rate of 2 per day or less.

At several steps during the assembly sequence, the module will be electrically tested, repeating the short functionality test. In order to be able to read out the hybrid, a short digital jumper cable (testing cable) needs to be connected to the module. This test cable can be installed for the initial

hybrid test and burn-in cycle and can remain in place through the module assembly process, in principle, although it may be preferable to remove this cable during attachment and bonding of the analog cable to the hybrid. The connection of this testing cable needs to be done by a skilled technician, as it is a delicate operation that takes place with exposed wire bonds. The testing cable will remain attached to the module during the complete testing process until the module is installed on the support structure and the final jumper cable is connected. Malfunctioning modules at any step of the assembly sequence will be sent to the repair team for diagnosis and repair. Module storage boxes have been designed which allow for electrical testing, providing a path out of the box for the digital readout cable, ports in the base for dry gas purge, cooling of the hybrids through the base plate of the box and a light-tight seal to allow biasing of the sensors. The modules will remain in these boxes through testing and burn-in and will only be removed when they are to be installed.

Completed modules will be sent to the debugging team to investigate their performance under HV bias. Pinholes could develop during wire bonding and can be addressed by pulling a wire bond between the AC sensor pad and the SVX4 chip preamplifier. Because all our silicon modules use single-sided silicon sensors, we expect the debugging of detector modules to be much less demanding than the one required by double-sided sensors. Once the detector module is operational under high voltage, it will be sent for module burn-in.

6.7 Debugging of Detector Modules

Immediately after a detector module is produced, and before it is burned-in, it needs to undergo a functionality test, that we call “debugging”. The likelihood of damaging the detector modules during construction, in particular during wirebonding, is not negligible. An intermediate step between production and before module burn-in is needed to restore the functionality of the modules before performing any electrical tests. The steps we plan to follow during the debugging process are the following.

- Visual Inspection: A thorough visual inspection of the finished module will ensure that no mistakes were made during wire bonding and no mechanical damage occurred.

- Functionality test: this test is done on the module without applying bias voltage to the sensor to assure the electrical integrity of the hybrid after module production.

- Biasing of the detector: bias voltage is applied in 5V increments, monitoring the leakage current. Capacitors that might be broken during wirebonding will be identified during this step. Strips corresponding to broken capacitors will be disconnected from the readout electronics by pulling a wirebond between the silicon sensor AC bonding pad and the SVX preamplifier.

- Characterize the module by producing V-I and V-noise curves and determining the operation voltage.

We plan to have two 1-Saseq debugging stations in the Lab D clean room to check out modules as soon as they have been completed.

6.8 Burn-in Tests for Hybrids and Detector Modules

The burn-in test is part and parcel of the testing procedure for module production. It will be performed first on the stuffed hybrid after it has passed the initial functionality test described above. At this point the hybrids are subjected to long term readout cycles. The goal of the test is to select good hybrids for module assembly. The second burn-in test will be carried out after a module has been produced and it has passed the initial functionality test. The idea of the burn-in test is to run every component for a long period of time (at least 72 hours) under conditions similar to those expected in the experiment and monitor its performance, in particular, measure pedestals, total noise, random noise and gain and examine occupancy in sparse readout mode. Other parameters that will be monitored include temperature, chip current, and detector bias voltage and dark current measurement (in module burn-in only). Typical problems that are revealed by the burn-in tests are SVX chip failures, broken and shorted bonds, grounding problems, noisy strips and coupling capacitor failures.

Both the hybrid and the module burn-in stations had been completed for the Run IIb silicon project and are fully functional and available for the Layer 0 project.

The burn-in software has been fully developed and is based on a user-friendly Graphical User Interface written in the TCL/TK scripting language with the graphical toolkit in the Windows environment. This choice of software interface created a flexible system for performing a variety of tests using executables written in different programming languages, for data taking, monitoring and data analysis.

The different tests performed during burn-in are the following:

- Temperature sensor test: performed at room temperature, before the SVX chip is powered.

- Data integrity check: tests the stability of downloading the SVX chip and verifies chip identification number (ID) and channel numbers of the SVX data for each chip.

- Long term burn-in test: it consists of a number of runs with an idle interval between them in which the chips remain powered. In each run, the SVX chips are tested in “read all” and “read neighbor” modes. In “read all” mode, chip pedestals are read out to evaluate the noise in each SVX channel and the chip calibration is performed. In sparse readout mode (“read neighbor"), where only the channels whose response exceeds the preset threshold and their immediate neighbors have to be read out, the frequency of false readouts is studied.

For detector modules, this test is performed with the module under bias. For a detailed description of the tests performed during burn-in in Run IIa, see DØ Note 3841. We plan to run the same tests during Run IIb.

6.9 QA Test for Detector Modules

Mechanically, all modules will be surveyed using the OGP, an optical CMM with pattern recognition that can quickly measure all of the fiducials on the sensors. This was done with the ladders in Run IIa. This measurement will also provide data on the flatness of the freestanding modules. We plan to subject a fraction of the detector modules to a thorough set of QA tests. The final set of tests will be developed once prototype modules are being produced. The current plan is to test modules in the following areas:

- Laser test: This test is meant to verify the response of the silicon sensor to a light signal. Detector modules will be placed on an X-Y movable table enclosed in a dark box, biased and illuminated with a highly-collimated pulsed IR laser, providing a detailed test of each strip of the detector module in a functional setting. The same system was used during Run IIa. It is based on a 1-Saseq test stand, with the addition of the movable table, dark box, and Laser. The solid state laser operates at a wavelength of 1064 nm, a wavelength chosen because the high resistivity silicon used in the detectors is partially transparent to it. The attenuation as a function of silicon thickness has been measured, resulting in an attenuation length of 206 μm. This laser will thus test the whole depth of the 320 μm thick detector and not just a surface layer. We plan to do a detailed scan of the modules to check for uneven response of the sensor to the laser.

- Temperature cycles: The cooling provided during burn-in is only meant to avoid mechanical and electrical damage to the modules. The modules will run at a temperature between 10 and 15 C. We consider that a detailed temperature cycle test, in which modules are read out and checked for mechanical integrity after being subject to temperatures of -10 C, is desired.

- Probe testing: We do have the ability to probe test silicon sensors after they were assembled into modules, or to do detailed checks of signals in the SVX chips by means of a logic analyzer and a probe tip. We can use this tools for QA tests if found appropriate once we gain experience during the pre-production phase.

- Pull Tests: we will test wire bonds on the hybrids and between hybrids and sensors on their pull strength during the pre-production phase, and might consider doing it in a small fraction of modules during production if needed.

6.10 Electrical Tests of Layer 0 Detector

We plan to perform two types of tests on the modules during final assembly of the Layer 0 detector. Both tests will be performed using a 3-Saseq test stand located in Lab C, close to the assembly stations. The first test will be performed on individual modules, immediately before and after mounting on the support structure. The second test will read out up to six modules simultaneously after installation, to check for cross talk and grounding problems. The steps of

the single module test will be specified following the procedure used during insertion of ladders into the Run IIa SMT bulkhead (see Ref. [29]), and are summarized below:

1. Temperature sensor check at room temperature: ensures that the temperature sensor on the module is working properly. This test is done before the chips are powered.
2. Download of SVX chips for data mode operation
3. Check channel and chip ID
4. Take 100 events in data mode. Check for uniformity of pedestals and noise level
5. Download of SVX chips for cal-inject mode operation
6. Take 100 events in cal-inject mode. Check for uniformity of pedestals and noise level
7. Bias the detector to the operation voltage (depletion voltage +5V)
8. Repeat steps 2 to 6

After six Layer 0 modules are installed on the support structure, they will be connected and read out simultaneously, to check for crosstalk and grounding problems. Cooling of the modules during assembly and testing will be done with water at 3 C. Details still need to be understood to minimize the number of times cooling is connected and disconnected during the assembly process.

6.11 Full System Electrical Test

All the tests described so far on stuffed hybrids and detector modules during production and assembly of the Layer 0 detector are performed using Stand-alone (Saseq) based test stands.

These tests are aimed at testing a large number of detector modules extensively and with redundancy in order to detect problems and fix them. The production testing needs to be complemented with a test of the real readout chain, the one that will eventually be used for the data acquisition in the experiment. This test is described below.

We plan to test the full readout chain with up to 8 modules or stuffed hybrids, through all of the components of the final readout chain, at the Fermilab Silicon Detector Facility. The goal of this test is to understand the full readout system and perform modifications well before the system needs to be operated in the collider. We will maintain one test stand that is capable of testing up to 8 hybrids. The setup includes all three types of crates participating in the SMT readout: an Interface Board crate, Sequencer crate and VRB crate. The High Voltage System and LV system will be integrated into the test stand as it becomes available. The DØ Trigger Framework functionality is replaced with a FPGA board that emulates those functions required. This allows us the flexibility of operating without the DØ trigger framework. Data will flow from the

[29] See http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/Testing/barrel_assembly.pdf

detectors to the SBC and then by Ethernet to a local LINUX based computer. The electronics can be controlled either by software based on Excel spreadsheets or by the Run IIa SMT online software. The Excel based software is currently used by the DØ engineers to debug the hardware while the online software provides a realistic test at full readout speed.

As we start receiving prototypes we plan to perform the following tests using this setup:

- Hybrid with SVX4 chips connected with Jumper Cable to the Purple test card and to the Sequencer. This test is complementary to similar tests with SASeqs. In addition it facilitates developing of all firmware changes for production Sequencers.

- Full readout chain: Hybrid – Jumper Cable – Junction Card – Twisted-Pair Cable – Adapter Card – 80-conductor cable – Interface Board – 50-conductor cable – Sequencer. These tests are crucial to verify the performance of all components. The timing studies are especially important to verify the impedance matching between different components and the signal terminations.

6.12 Production Database

All information relevant to the production and testing effort will be kept in a production database already developed for the Run IIb project. For the design of this database, we're following the description of the ATLAS Silicon Tracker production database[30]. Each item (hybrid, sensor, module, etc.) has its unique ID for easy identification and tracking. In addition, we provide a web-based interface to the database so that vendors and remote institutions can easily upload their testing information to a central location.

[30] http://www.hep.man.ac.uk/groups/atlas/SCTdatabase/Database.html

7 RADIATION AND TEMPERATURE MONITORING

All silicon detectors will eventually be rendered inoperable or develop inferior performance due to the effects of radiation. The effects of radiation damage can be minimized by maintaining an operating temperature of the silicon sensors of near of below 0 C. For the DØ SMT detector, the front-end readout electronics are mounted near the silicon sensors, so the danger of excessive heat and possible thermal run-away is always present. Without adequate cooling, the energy dissipation in the front-end electronics could swiftly render the detector useless for physics. Less extreme heating, while not causing catastrophic damage, can greatly exacerbate the effects of radiation damage. Careful monitoring of temperature and radiation dose is therefore crucial to the safe and reliable operation of the detector. In Run IIa, currents, temperatures, voltages, and radiation dose from the accelerator are all monitored and interlocked at several levels. Some modest improvements are planned for the radiation and temperature monitoring systems for the Layer 0 silicon detector, as described below.

7.1 Radiation Monitoring and Beam Abort System

7.1.1 The Run IIa system

A radiation monitoring and beam abort system is currently in operation for Run IIa. This system consists of two independent subsystems: a system based on the Beam Loss Monitors as they are used by the FNAL beams division, and a system based on silicon diode sensors mounted directly on the detector. Both systems are independent up to a last stage, where the output of both are recorded in the same data stream and where a combination of the information of both systems can be made to trigger a Tevatron beam abort.

The Beam Loss Monitor (BLM) System consists of two sets of four glass cylinders filled with 1 bar Ar gas. On either side (north and south) four BLMs are placed at 3, 6, 9 and 12 o'clock positions around the beam tube, inside the shielding of the forward muon chambers. Radially they are about 12 cm away as measured from the nominal beam position to the center of the BLM tubes. Their position along the beam direction is about 4 m from the nominal average interaction point. The position of the BLMs is sketched in Figure 81.

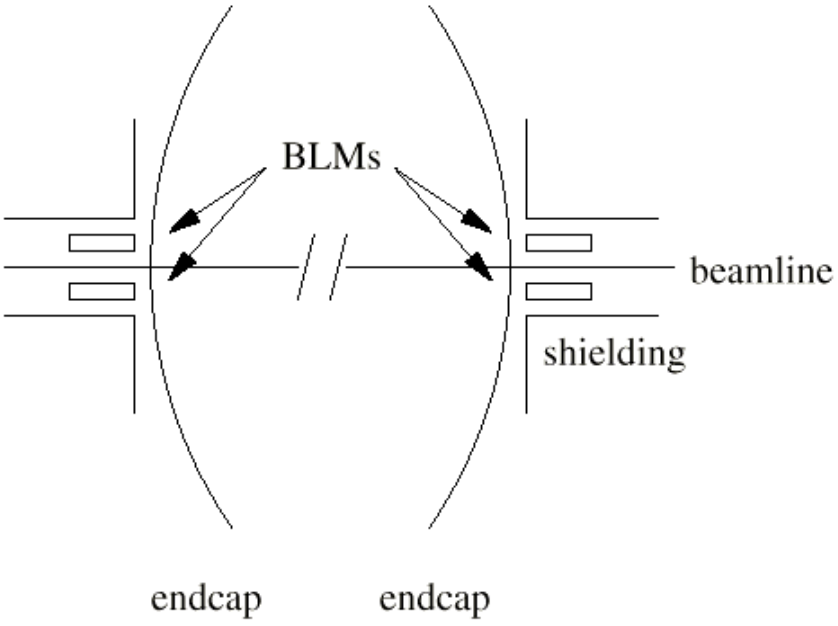


Figure 81 - Location of Beam Loss Monitors.

The dark current of these devices is extremely low, allowing sensitivity down to the single particle level. Currently the output signal is connected to standard beam division electronics C336 modules, which functionally consists of a slow (0.94 s time constant) logarithmic integrating circuit. The processed signal is also fed into a C335 discriminator module that triggers the Tevatron beam abort.

Because of their position relatively far away from the interaction point and the SMT, the BLM system does not necessarily give the correct indication of the radiation levels at the SMT. Nevertheless, a large fraction of the times that excess radiation was observed, the time structures of the levels recorded from the BLMs and the silicon diode sensors were similar.

The Silicon Diode Sensor System devices are also known as the radiation monitoring fingers (radmon fingers), because of the shape of the sensor boards. The front-end sensor boards are finger shaped to fit in between the F-disk modules and H-disk modules of the current SMT. On both the north and south side of the experiment, six radmon fingers are mounted on the outer F-disk plane (F-disks 1 and 6) and on the outer H-disk planes (H-disks 1 and 4). A picture of one of the fingers is given in Figure 82.

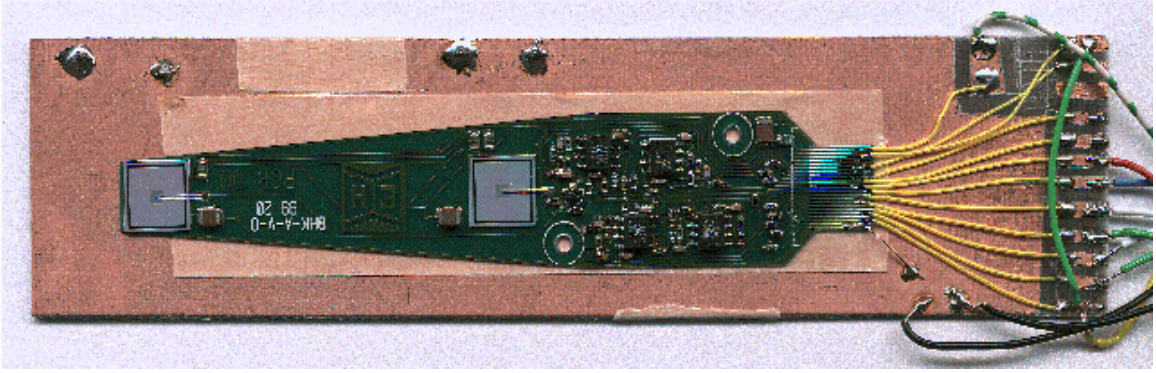


Figure 82 - Radiation monitor finger.

The fingers each contain two diodes that are read out individually and are placed at different radii. The radii of the diode positions are arranged such that the inner H-disk diodes are at the same radius from the beam as the outer F-disk diodes. The inner F-disk diodes are at radius 2.6 cm from the beam, the outer F-disk and inner H-disk are 9.5 cm from the beam, and the outer H-disk diodes are 16.5 cm from the beam position. In the direction along the beam the F-disk fingers are located at 55 cm from the average interaction point, and the H-disk fingers are at 120 cm. The mounting on the F-disks is shown in Figure 83.

Figure 83 - Mounting of radiation monitor fingers on F-disks.

The signal from the silicon diodes is pre-amplified locally on the diode card with two different gains to increase the dynamic range. The electronics has only one type of amplifier as the active component, and this amplifier was chosen specifically for its radiation hardness (at least several MRads) and its large gain-bandwidth product (about 1 GHz). To be sensitive to even a single minimum-ionizing particle passing through the diodes, scalars are connected to the channels which count pulses above a set threshold. This allows measurement down to a rate of a few microRad/s. The saturation level of the low gain amplifier channel is about 25kRad, hence the dynamic range of the system is about 10 orders of magnitude.

The diode boards are mounted such that they have very good thermal contact to the cooling ring of the F-disk. Because the dissipation of the diode cards is small, they maintain a significantly lower temperature than the F-disk modules and are therefore expected to survive a higher radiation dose than the SMT itself. In addition the electronics is set up such that large leakage currents that may flow into the amplifier can be compensated externally from the counting house. By adjusting the compensating current, several mA can be taken out of the diodes, corresponding to a radiation level at which the SMT itself will have died. To keep the diodes depleted, even after radiation damage, the system allows a bias voltage up to 300 V.

Calculations indicate that a minimum-ionizing particle passing through the silicon diodes should produce a signal of about 30 mV. This value is confirmed by calibrations done in situ in the Tevatron, comparing beam-on and beam-off conditions.

As a qualitative cross check of both BLM and silicon diodes, we normally see that the radiation dose rates on the BLMs and the diode sensors track in time. However, the relative normalization varies, indicating that the mechanisms of radiation loss are not always the same. An example of signals recorded from the silicon diodes in a mild radiation incident is shown in Figure 84. This figure shows that the dose rate as estimated from the scaler counting rate and the dose rate as measured through the shaping and integration circuit have good qualitative and quantitative correspondence, up to an uncertainty of about 10% in absolute calibration.

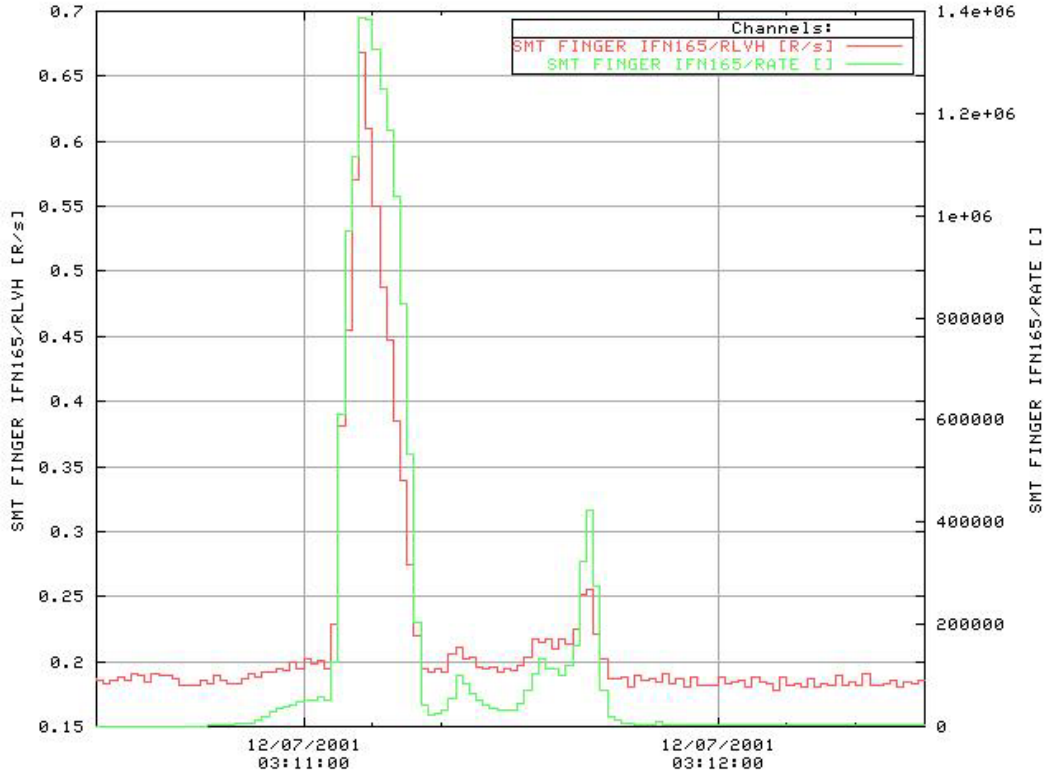


Figure 84 - Dose rate from a single radiation monitor finger as measured by both the scaler rates and from the integration and shaping

7.1.2 The DØ Layer 0 radiation monitoring system

The BLM system will be maintained as it is. This system is very reliable and radiation hard, so there is no need to replace it. Also the silicon diode sensor system is expected to continue to perform well, so we do not plan to replace it.

In the Run IIa system we can clearly see the detector readout signals as noise in the silicon diode readout. Although the noise level is not jeopardizing the system, we think we can reduce it. The main area where the noise couples in is thought to be either the sensor board itself, which is very close to the F-disk modules, or the low mass HDI cables which are packed together with similar low mass F-disk module cables. We will explore methods of improved grounding and shielding to reduce this readout noise.

7.2 Temperature Monitoring

Due to the proximity of much of the electronics to the silicon sensors, temperature monitoring of the detector is crucial. Remote-sensing devices mounted on or near the sensors themselves are needed to continuously monitor temperatures and to provide interlocks to shut off power in the event of a loss of cooling or other problem. The temperature-sensing device of choice is a Resistance Temperature Detector (RTD), a thin-film platinum resistor with a high temperature coefficient of resistance. These devices are widely used in industry and are known to be stable, reliable, and radiation hard.

7.2.1 Run IIa temperature monitoring

In the Run IIa SMT, the temperature of each High Density Interconnect (HDI) is monitored with an RTD. There are about 900 RTDs in the Run IIa silicon system. They are read out through a two-wire system in which the same leads both supply a DC current and read out the resulting voltage. This readout method, which does not compensate for the resistance of the leads, limits the accuracy to about 2 to 3 C. The analog voltage signal (a DC voltage level) goes to the Interface Board, where it is digitized and read out serially to the 1553 monitoring system. The reading from each RTD is interlocked so that if the temperature goes above 15 C, the power to the appropriate HDI (only) is tripped.

In addition to the temperature monitor on each HDI, 88 of these signals have a second readout. An analog signal is taken off the Interface Cards before digitization and read out through an ADC in the DØ Cryo Control System, which is a Programmable Controller (PLC), a commercial system widely used in industry for monitoring and interlocks. The 88 RTDs read out in this way serve as one of several signals that interlock power to the entire silicon system. The Cryo Control System serves as a redundant system to the 1553 interlocks, and is on a UPS so it would still function in the case of a power outage.

7.2.2 Layer 0 temperature monitoring

For the DØ Layer 0 silicon, two temperature monitoring systems will be in place. The system that interlocks the current in each HDI will be reproduced. For Layer 0, the HDIs are replaced by hybrids. Each hybrid will have an RTD mounted as one of the elements. The devices chosen are Honeywell HEL-700 1000 Ω platinum thin-film RTDs. Signals from each of these RTDs will be digitized on the Interface Card and read out through the 1553 as is currently done for Run IIa. The temperature monitors on each hybrid will be used to interlock the power of that individual hybrid.

For Layer 0, there will be a second temperature-monitoring system which will be decoupled from the hybrids. This system will provide accurate monitoring of Layer 0, as well as improved monitoring of the entire SMT cooling system. RTDs will be mounted at various locations on the sensors, electronics, and cooling system. RTDs mounted inside the detector will be read out through low-mass kapton flex cables which will extend to the junction-card region, where they will be connected to higher-mass cables which carry the signals to the horseshoe region. A commercially-available module, the CTI505, model 2557-SPQ334, from Control Technology Incorporated, will be used to both provide the activation current to the RTDs and readout the resulting voltages. A prototype module, designed specifically for these RTDs and this application, has been designed by CTI, is in hand, and has been tested. The CTI module's four-wire readout will have an accuracy of 0.5° C or better, compared to the current accuracy of 2 to 3° C. This improved accuracy should provide better understanding of the entire DØ SMT cooling system.

This stand-alone system will be part of the DØ Cryo Controls System, which will provide for appropriate interlocks and data archiving. The temperature sensors will be mounted on or near the sensors, so the information will directly reflect the actual sensor temperature. The two temperature monitoring systems together provide necessary redundancy for adequate protection against failures of the cooling system.

8 SOFTWARE

The software needed for commissioning and online calibration, monitoring and readout of the Layer 0 detector is not any different from the software needed for the Run IIb detector. For both offline and online software effort, we will use the system developed for Run IIa and upgrade it appropriately for Run IIb where needed. For brevity, we refer for a full description of the software needed to the Technical Design Report we submitted for the Run IIb silicon detector.[31]

[31] DØ Run IIb Upgrade Technical Design Report, FERMILAB-PUB-02-327-E, December 2002.

9 SIMULATION OF THE LAYER 0 DETECTOR PERFORMANCE

9.1 Overview

Given the very short time scale for this proposal, it was not possible to perform studies of the performance of the tracker with the addition of the Layer 0 detector using a full GEANT simulation and reconstruction code. We have relied on studies performed previously for different detector configurations. We believe that most of our conclusions are still applicable to the proposed detector configuration. Pattern recognition studies were done about 3 years ago when DØ was considering a partial replacement option for the current silicon microstrip tracker. A somewhat different Layer 0 geometry was considered at the time – 12-fold with 50 μm pitch silicon sensors. The pattern recognition code has significantly improved since then. Still we believe that our conclusion that Layer 0 will help to restore the pattern recognition capabilities of DØ detector is valid. Impact parameter resolution studies are done using a current Layer 0 geometry implemented in a parameterized model. A comparison with DØ data yields a good agreement giving us confidence in our results.

9.2 Occupancy

We have not performed occupancy studies with the latest geometry, but believe that most conclusions drawn in the Run IIb Technical Design Report are still valid. In that study, the two sublayers of the L0 detectors had silicon sensors at radii of 1.78 and 2.47 cm, and each sensor was 7.94 cm long, and had 256 readout channels with intermediate strips. The mean Layer 0 occupancy was found to be 4.5% in W-Higgs events with a rather low ADC threshold of 2.1 counts. As illustrated in Figure 85, the peak occupancy (maximum occupancy per ladder in an event) was about 10%. The addition of 6 minimum bias event increases the peak occupancy to 12%.

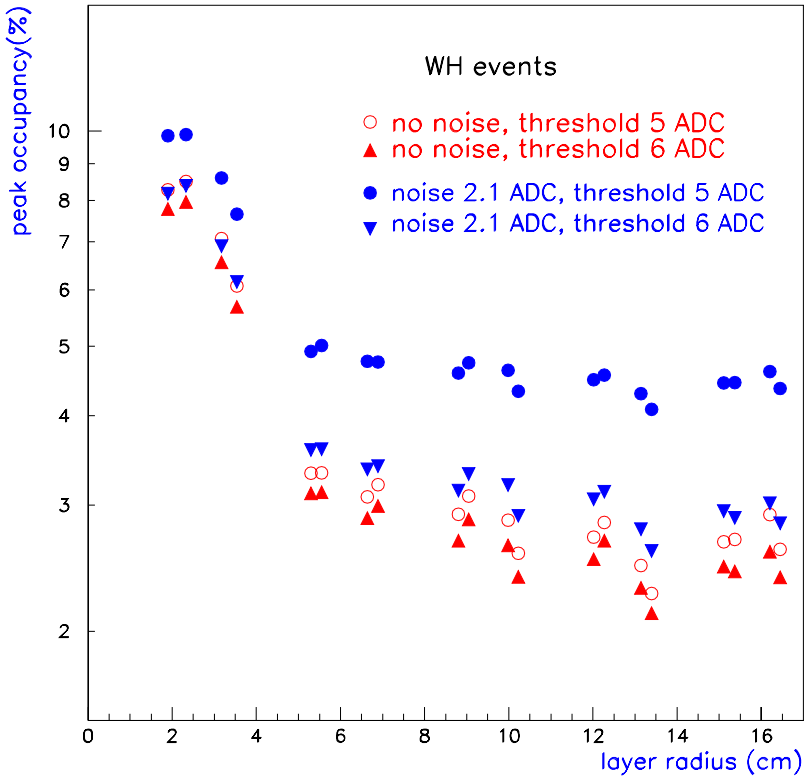


Figure 85 - Peak occupancy as a function of radius in W-Higgs events based upon a simulation study for the Run IIb silicon detector.

9.3 Pattern Recognition with Layer 0

We have compared the track finding efficiency of the DØ baseline detector with that of DØ with a fully inefficient L1, and then with L0 added but L1 fully inefficient, as might be the case after Layer 0 is installed (see Figure 86). In the central region where pattern recognition relies mostly on the fiber tracker system, the loss of L1 does not change the performance significantly, but for higher pseudorapidity regions (>1.6), the loss of L1 will cause significant deterioration of performance. The addition of the L0 detector restores the pattern recognition functionality, even though it provides only axial measurements.

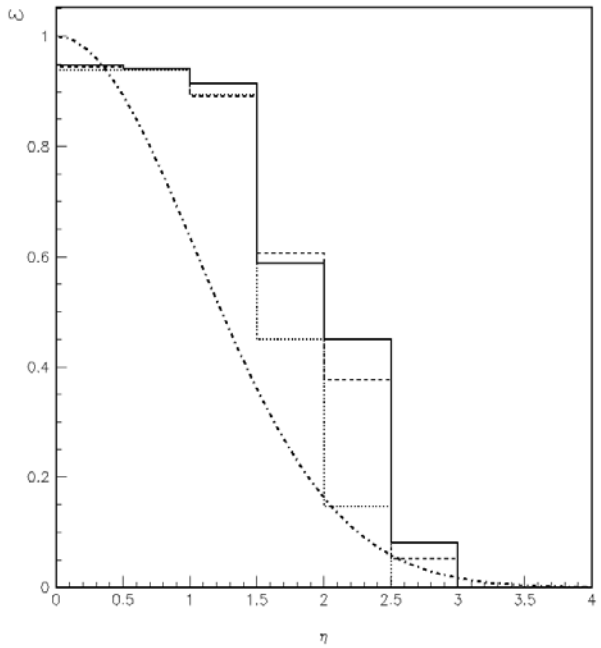


Figure 86 - Track finding efficiency of the DØ silicon detector, with and without L0, as a function of pseudorapidity η. The dot-dash curve shows a typical distribution of top-quark decay products. It has been ***assumed that the F-disks are nonfunctional in any of these scenarios.*** *The solid histogram shows the performance of the DØ baseline detector before radiation damage to L1. The dotted histogram shows the degradation in performance for higher pseudorapidity when L1 becomes nonfunctional. The dashed histogram shows that addition of a L0 detector restores nearly all of the lost pattern recognition capabilities.*

9.4 Impact Parameter Resolution with Layer 0

A parameterized model of the detector geometry was employed to investigate the effect of the proposed Layer 0 detector upon the impact parameter resolution of the tracker. As shown in Figure 87, the addition of the Layer 0 detector will provide a substantial improvement in the impact parameter resolution for tracks with low transverse momentum. Improved impact parameter resolution should result in increased efficiency for tagging b-jets, and potentially provide access to additional physics (see Section 9.6).

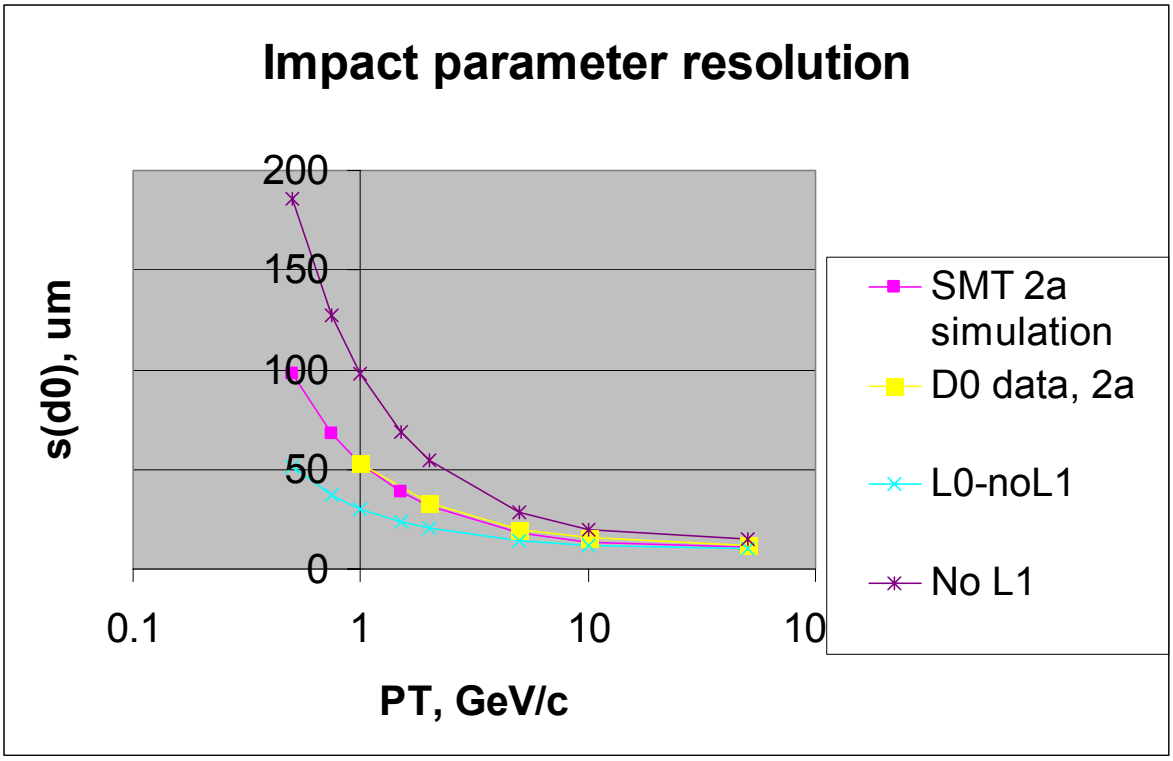


Figure 87 - Impact parameter resolution as a function of transverse momentum. Magenta curve: Present baseline DØ SMT, before radiation damage, yellow points – DØ data. Purple curve: DØ SMT after L1 becomes nonfunctional. Blue curve: After Layer 0 is added. Layer 0 provides a substantial improvement in impact parameter resolution.

9.5 B Tagging Efficiency

The sensitivity of the b-jet tagging efficiency of the current silicon microstrip tracker to potential changes in the performance of the tracker due to radiation damage and/or readout failures is illustrated in Figure 88, which shows the simulated b-tagging efficiency as a function of the pseudorapidity of the jet for the Run IIa tracker prior to irradiation (blue points), "after irradiation" (red points), and "after total loss of L1" (fuschia points). The "after irradiation" condition is implemented as 50% hits lost in L1 and the F-disks and 10% hits lost in the outer layers. The "after total loss of L1" condition is implemented as 100% hit loss in L1 and 50% hit loss in the F-disks. The b-jet tagging efficiency drops by a factor of 0.805 "after irradation", and by a factor of 0.636 "after total loss of L1". It is anticipated that the b-jet tagging efficiency lost due to radiation damage to the silicon microstrip tracker and aging effects would be recovered via the introduction of the Layer 0 detector.

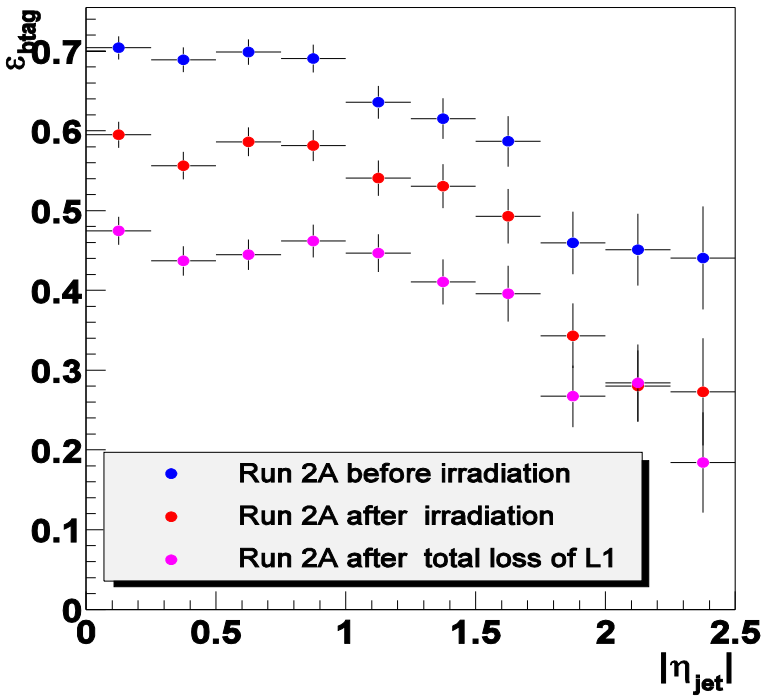


Figure 88 – b-jet tagging efficiency as a function of pseudorapidity

9.6 Layer 0 and B_s Mixing

This subsection briefly summarizes the impact of the Layer 0 detector on measurements of B_s oscillations. The short time frame for this proposal did not allow for dedicated studies to be performed by the time of this submission. In the following, we will assume some reasonable inputs for the proper time resolution, efficiency and dilution factors. A detailed investigation of these parameters is in progress in the DØ *B*-physics group both for the data and simulations.

The Tevatron experiments are in the unique position to investigate the physics of B_s mesons which are not produced at *B*-factories. Measurement of the frequency of B_s oscillations will provide a precise determination of the V_{ts} element of the three-generation Cabibbo-Kobayashi-Maskawa matrix. This will be a crucial test of the Unitarity Triangle parameters predicted by the Standard Model. The current limits imply fast oscillations of the B_s meson flavor with a period much smaller than the lifetime of the meson. A precise measurement of the frequency can be done resolving the time evolution of the oscillations. Figure 89 shows an example of simulated signal for the expected value of $x_B = \Delta m_s / \Gamma = 30.03$. The asymmetry $(N_{B_s^0} - N_{\overline{B}_s^0})/(N_{B_s^0} + N_{\overline{B}_s^0})$ is shown as function of number of proper lifetimes. As one can see,

good proper time resolution is of paramount importance to resolve the fast oscillations of the B_s asymmetry.

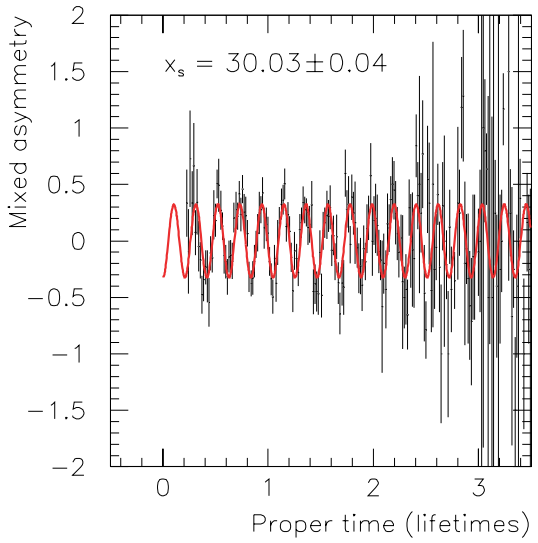


Figure 89 - Simulated B_s asymmetry as a function of proper lifetimes for x=30.03

Figure 90 shows an estimation of potential reach for the Δm_s parameter for various integrated luminosities. The plot compares improvements from two possible upgrades: the Layer 0 detector and increasing the Level 3 bandwidth by 50 Hz. The two green curves correspond to improved proper time resolution from the Layer 0 silicon detector without (dashed curve) and with (solid curve) the additional 50 Hz Level 3 trigger bandwidth. We assumed improvement in the resolution from 150 fs to 75 fs. The $B_s \to D_s \pi$ decay mode has been used for the estimate under the assumption that the events were triggered by leptons providing the flavor tagging. While the exact improvement of the proper time resolution coming from the Layer 0 detector still needs to be understood, it is clear that improved resolution has a dramatic effect on the reach of the Δm_s measurement. In this example, for one fb^{-1} of integrated luminosity the reach is increased from 16 to 24 ps^{-1}.

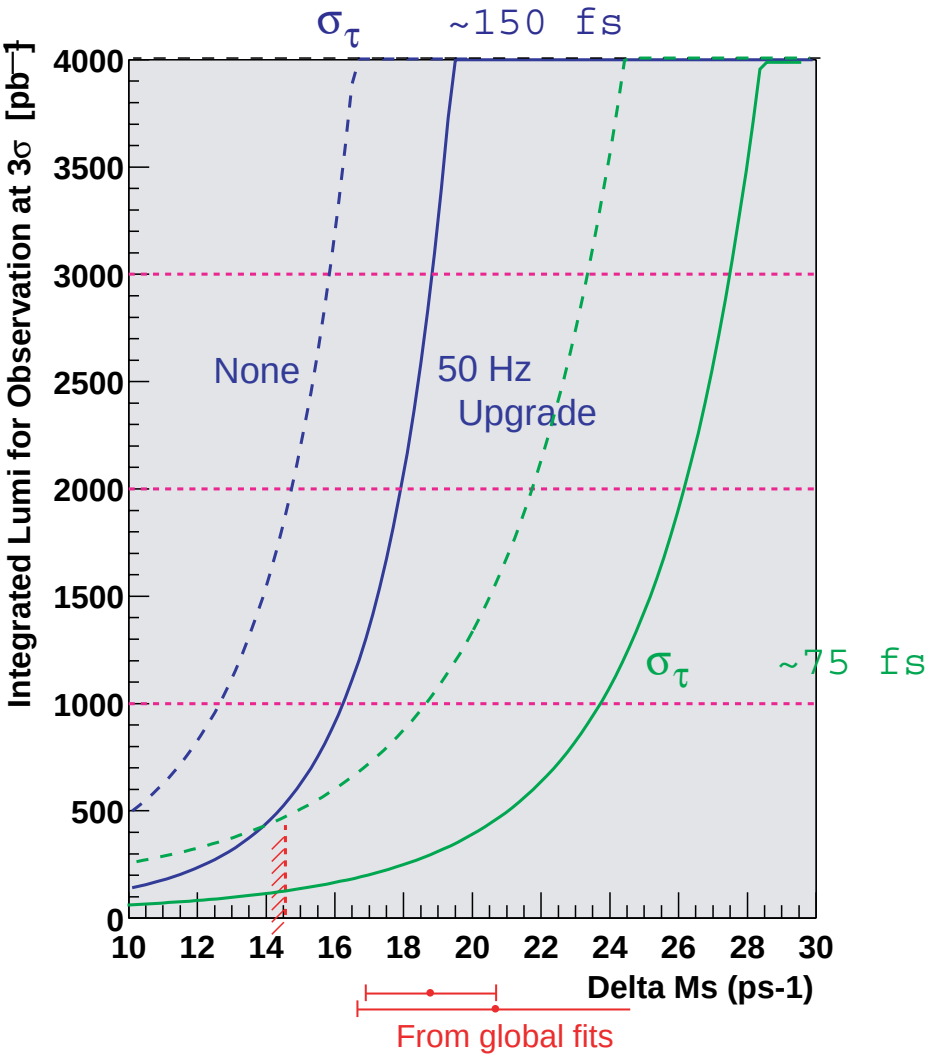


Figure 90 - Impact of improved resolution and trigger bandwidth upon the anticipated sensitivity to Δm_s versus integrated luminosity. The difference between the two dashed curves shows the improved reach in Δm_s attributable to improved resolution.

Thus the impact of the Layer 0 detector on the B_s mixing measurement is considerable and this represents another strong physics motivation for this Layer 0 silicon detector upgrade.

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